Diversified Technologies for System-on-Chip

Polytechnique, 9 March, 2004

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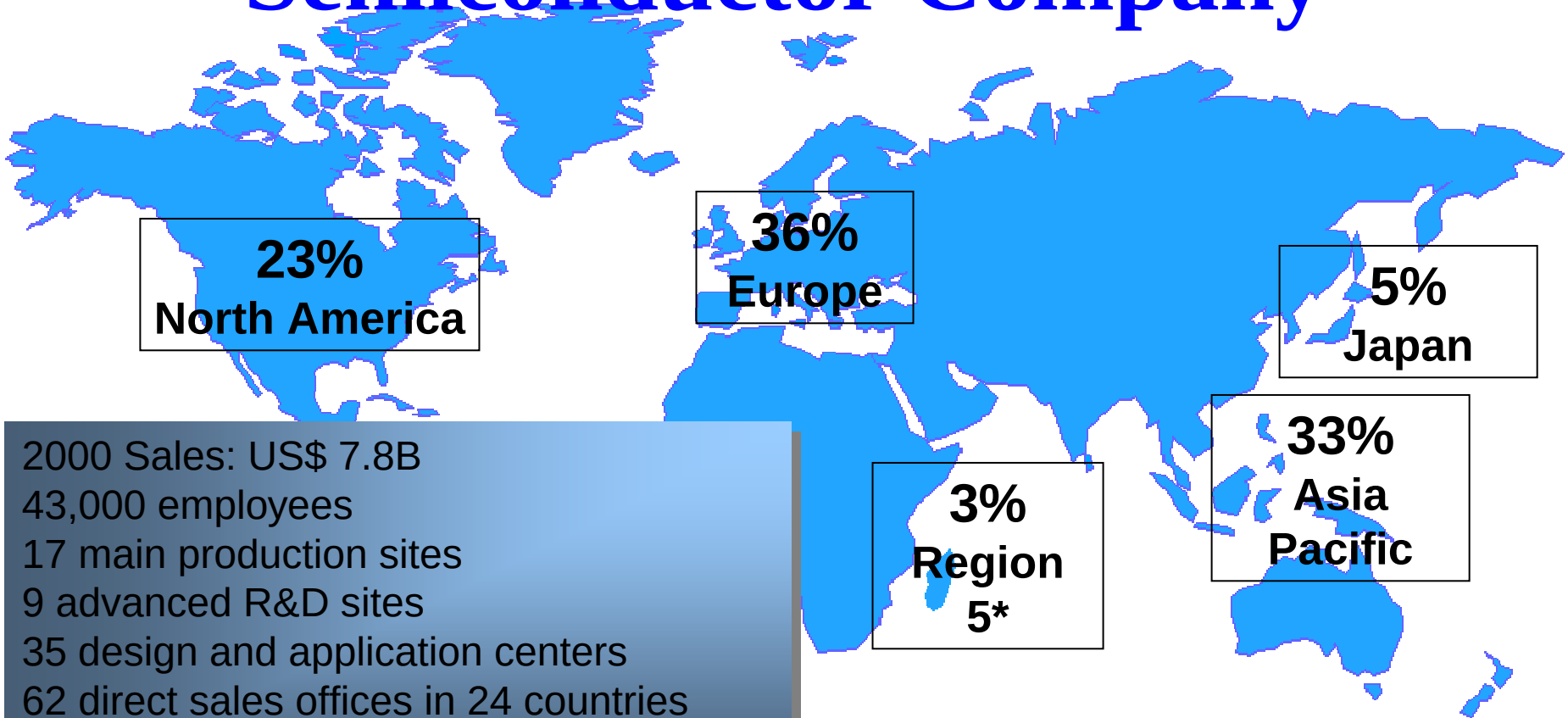
Agenda

- **The Market trends**
- **CMOS roadmap and added-value options**
- **Technology support for Low-power**
  - Optimized MOS, multi-Vt
  - SOI
  - eDRAM
- **Design / Manufacturing links**
- **System On Chip Design Challenges**
- **Competition.**
- **Conclusions**

SMicroelectronics - A Global Semiconductor Company



2000 Sales: US$ 7.8B
43,000 employees
17 main production sites
9 advanced R&D sites
35 design and application centers
62 direct sales offices in 24 countries
3th* largest semiconductor supplier
(*source Dataquest)

* Emerging markets

Les prochains defis de l'industrie de la microelectronique

- **Des defis d'ordre technique**
  - Technologie Nanometre
  - Systeme sur silicium
- **Des defis d'ordre economique**
  - Alliance
  - co-competition

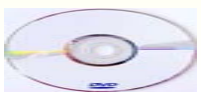
The market trends

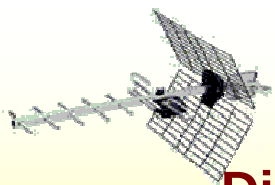
Living-Room Appliances




Satellite

DVD





Dig Terrestrial

Cable

ONE PLATFORM

Video Out

Audio Out

DVD – Variety of Applications

DVD TV Combos

Basic DVD Player

Personal DVD

DVD Audio

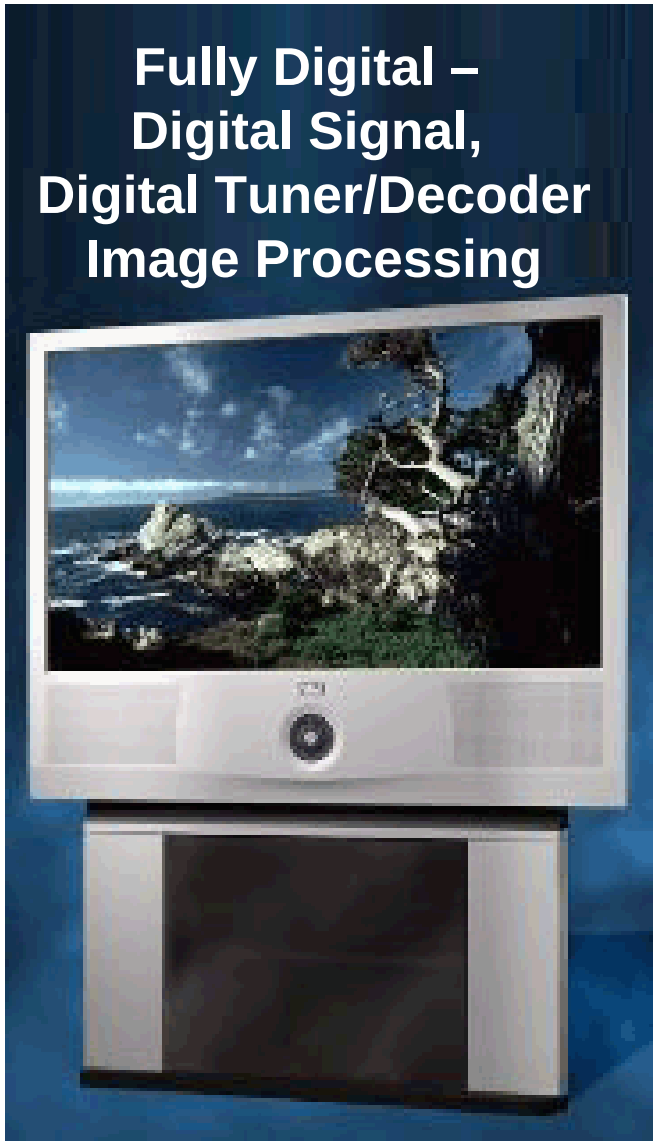
In Car Navigation

DVD Recorder

DVD Receivers

Migration of Digital TV

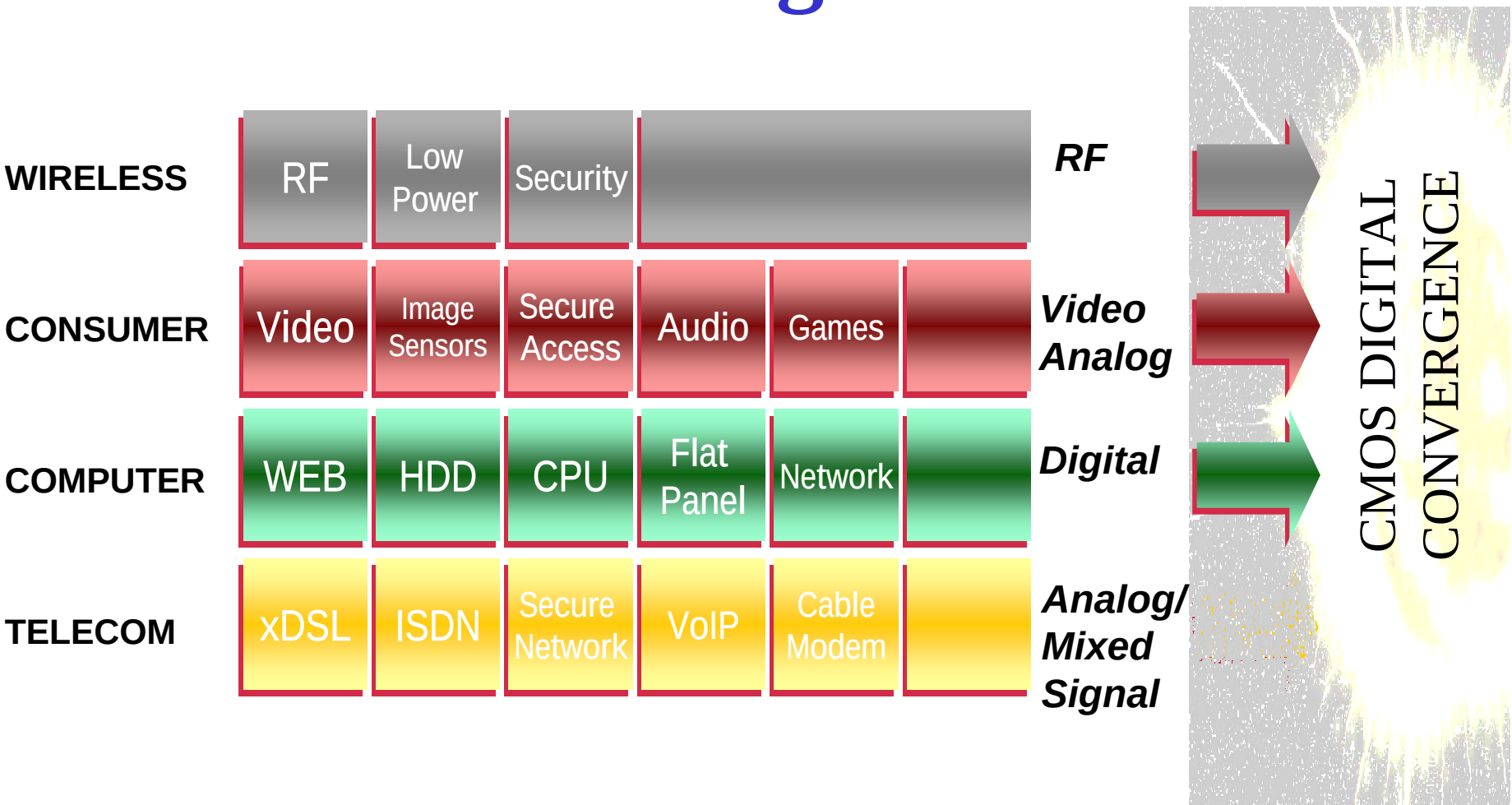
Analog Signals
+
Digital Image Processing



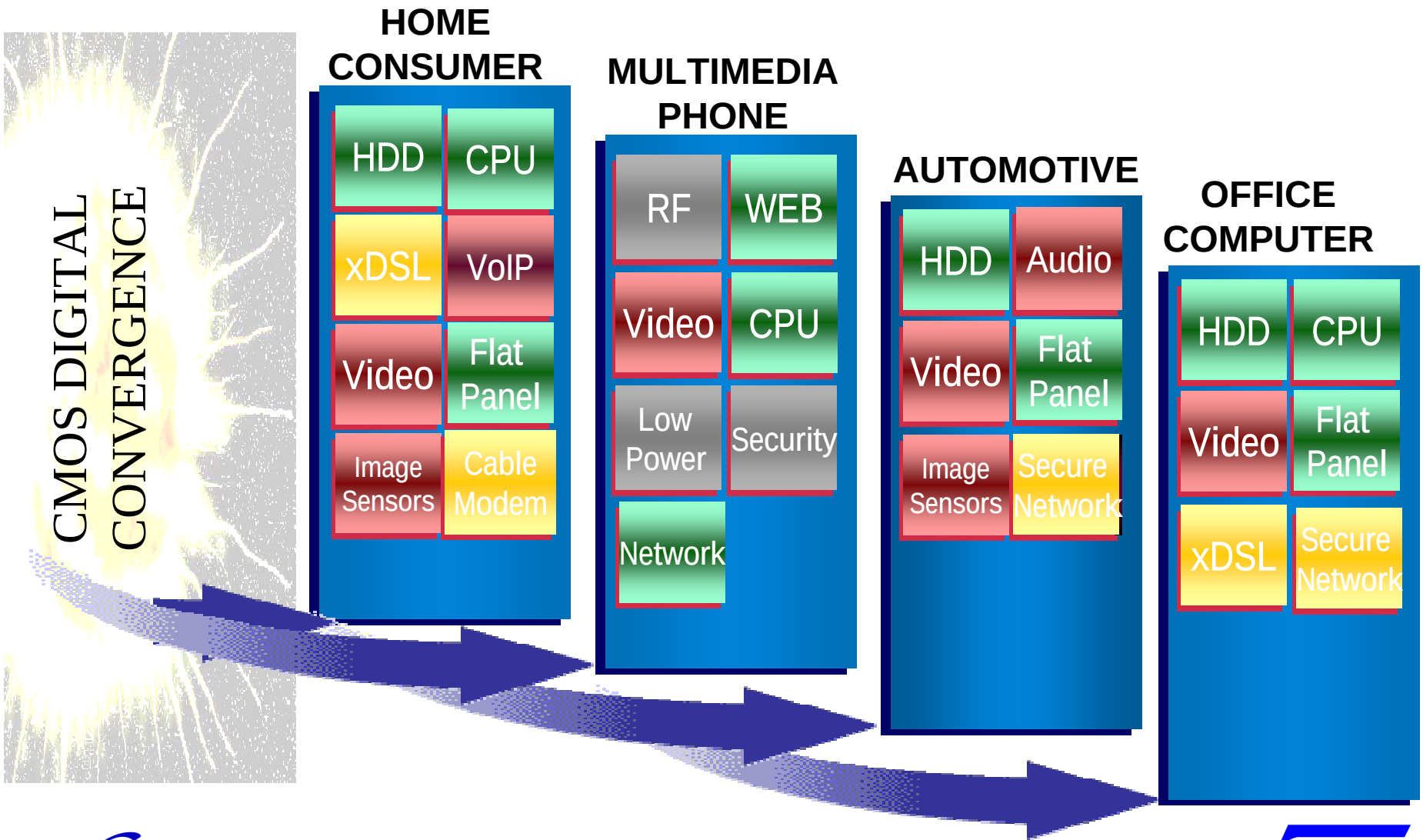
Analog TV
+
Free to Air
Digital Decoder
Terrestrial
Tuner

Home Network

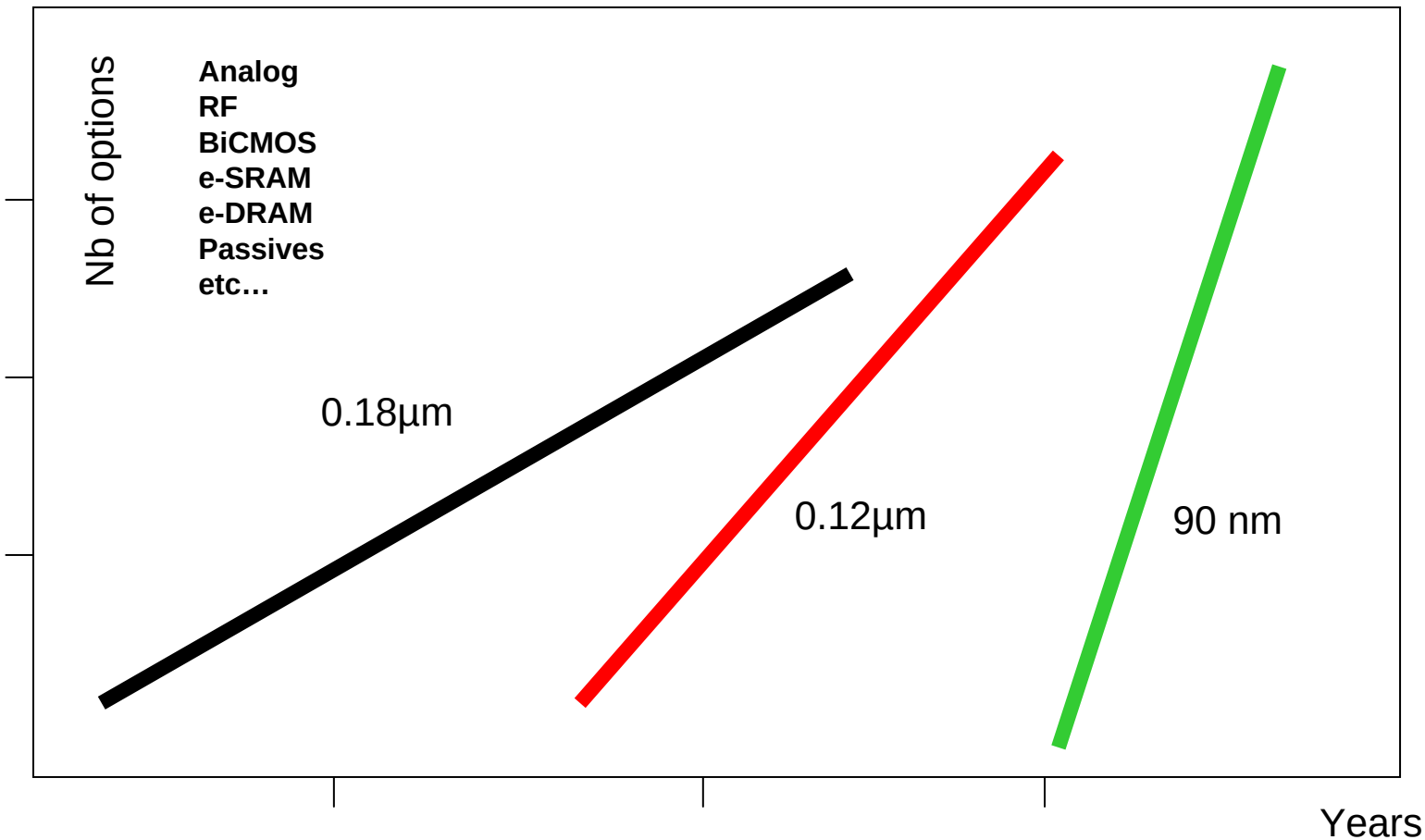
Convergence of Technologies…



…Divergence of Applications



More Options in shorter time

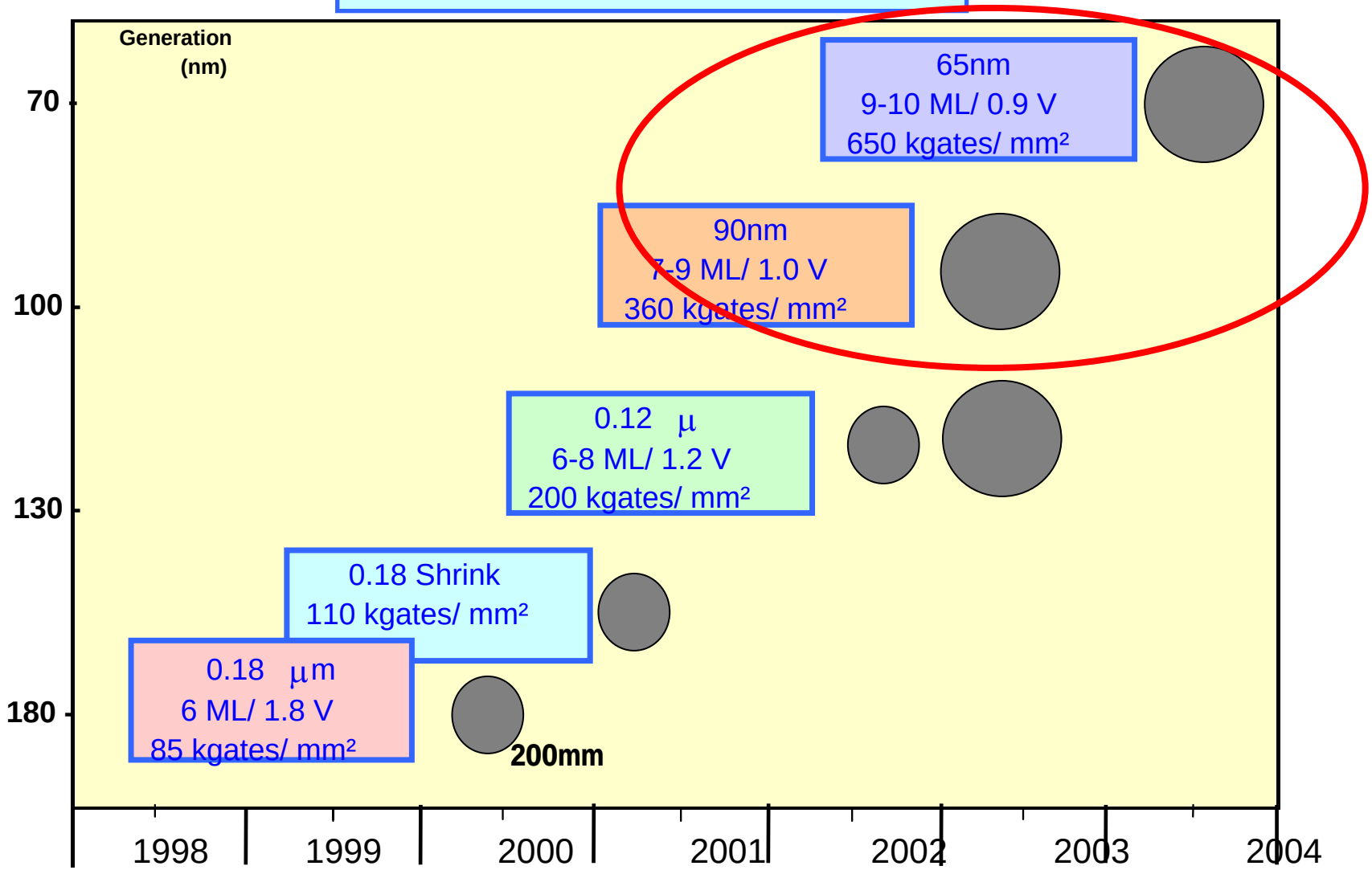


High Performance Technologies for …

- Very Low power consumption in SoC and also…
- Ultra Low noise RF performance
- High Speed digital and analogue (SiGe)
- Refined Analogue precision
- Energy Management (high voltage)
- High Density Memories (eDRAM, MRAM, Flash)

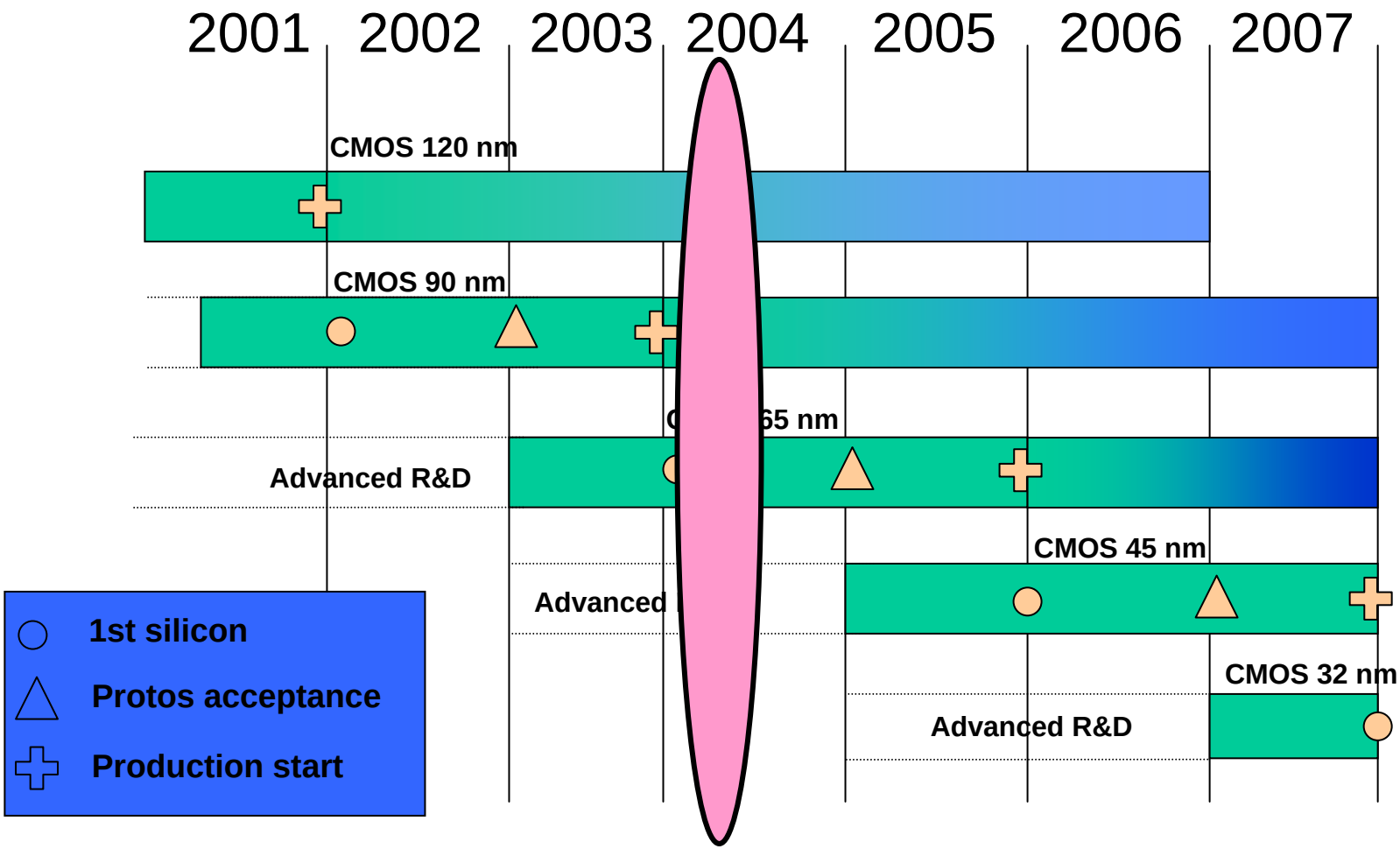
CMOS roadmap and added-value options

CMOS roadmap



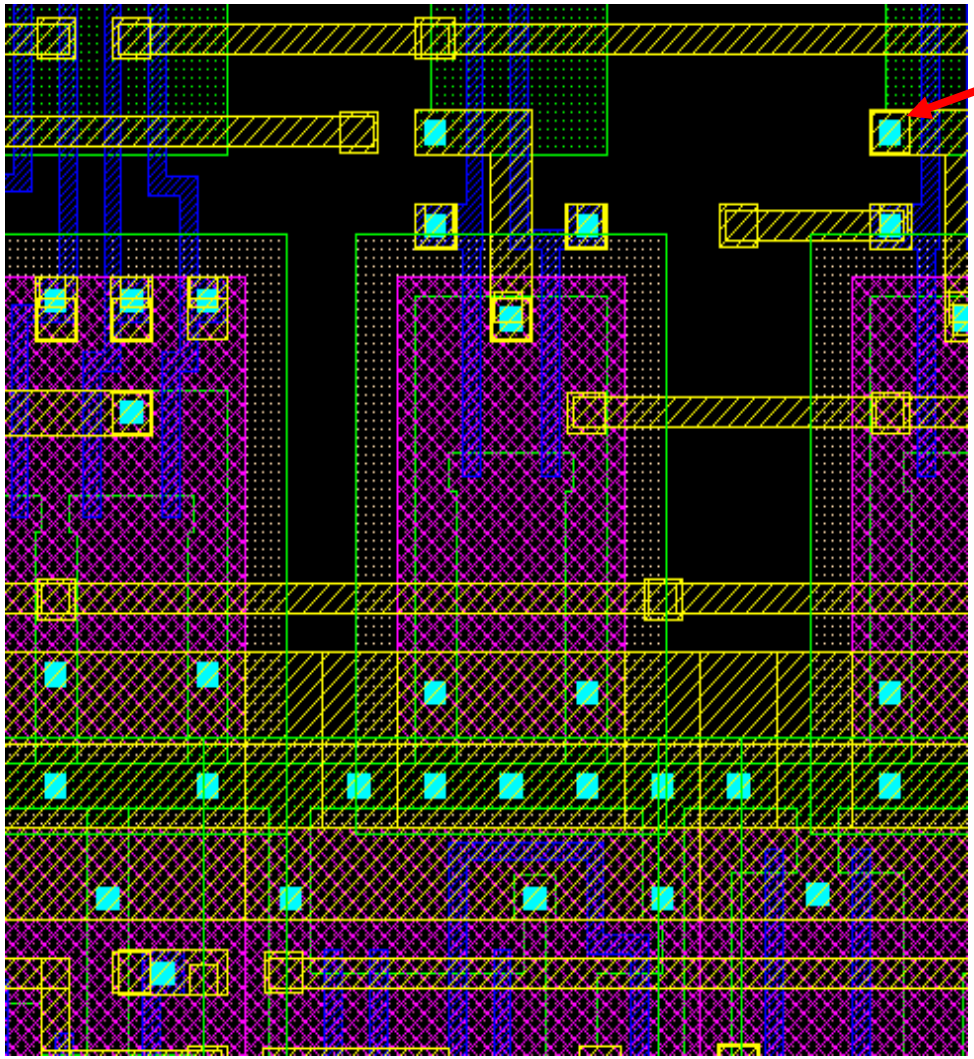
Right edge of boxes is PG acceptance

CMOS Roadmap: from R&D to production



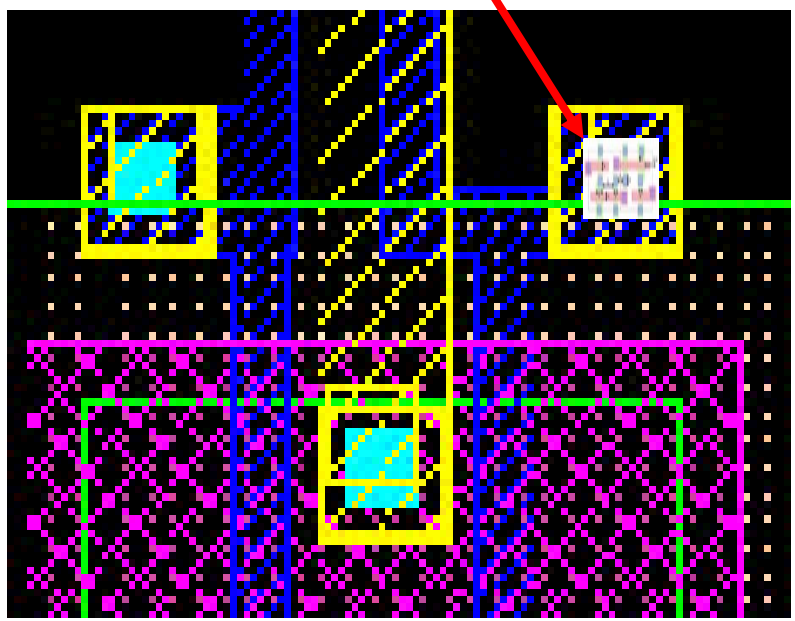
4 advanced CMOS platforms developed in parallel

Evolution in the last 10 years



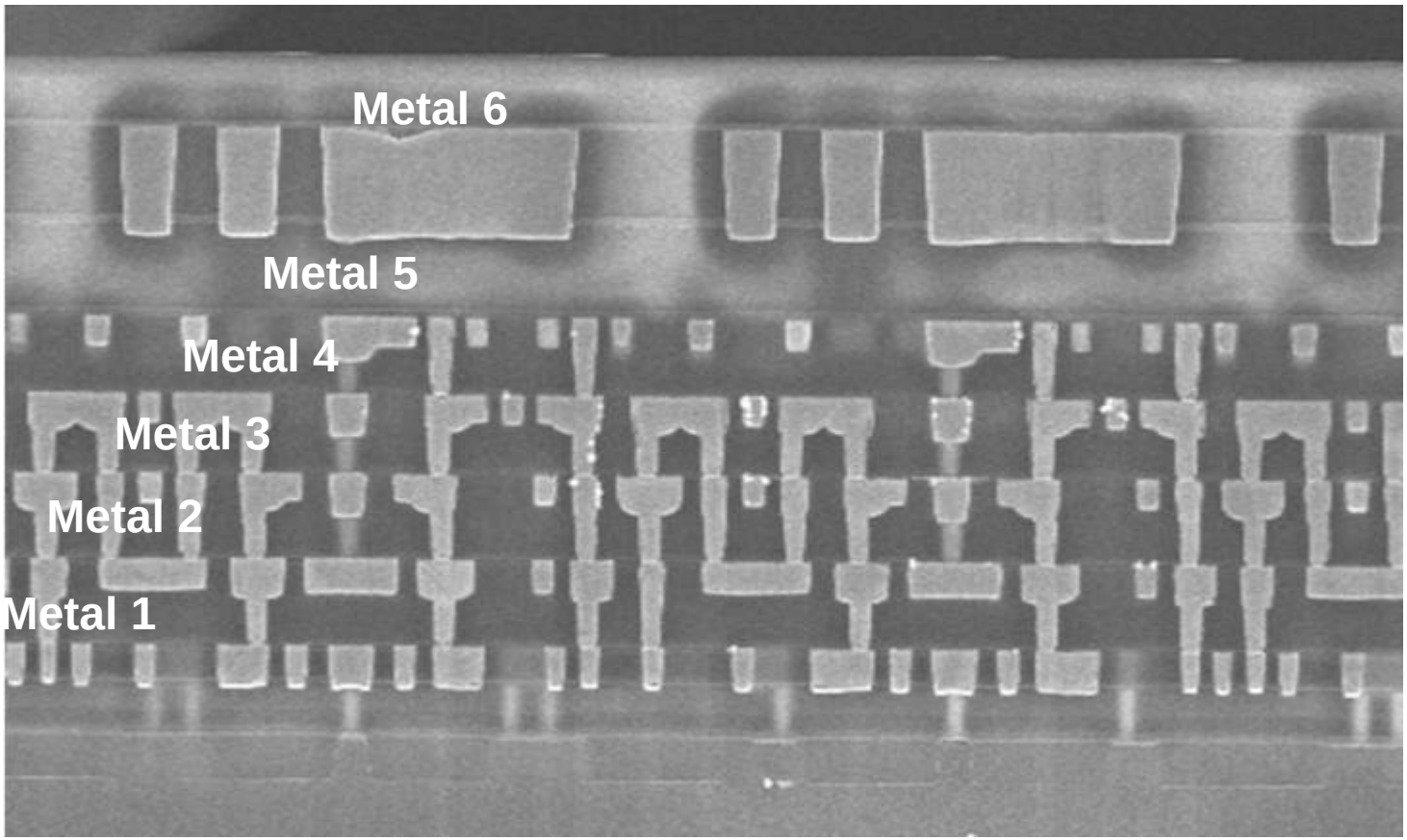
Contact in 0.5µm = 0.64µm2

6-transistor SRAM cell in 65nm

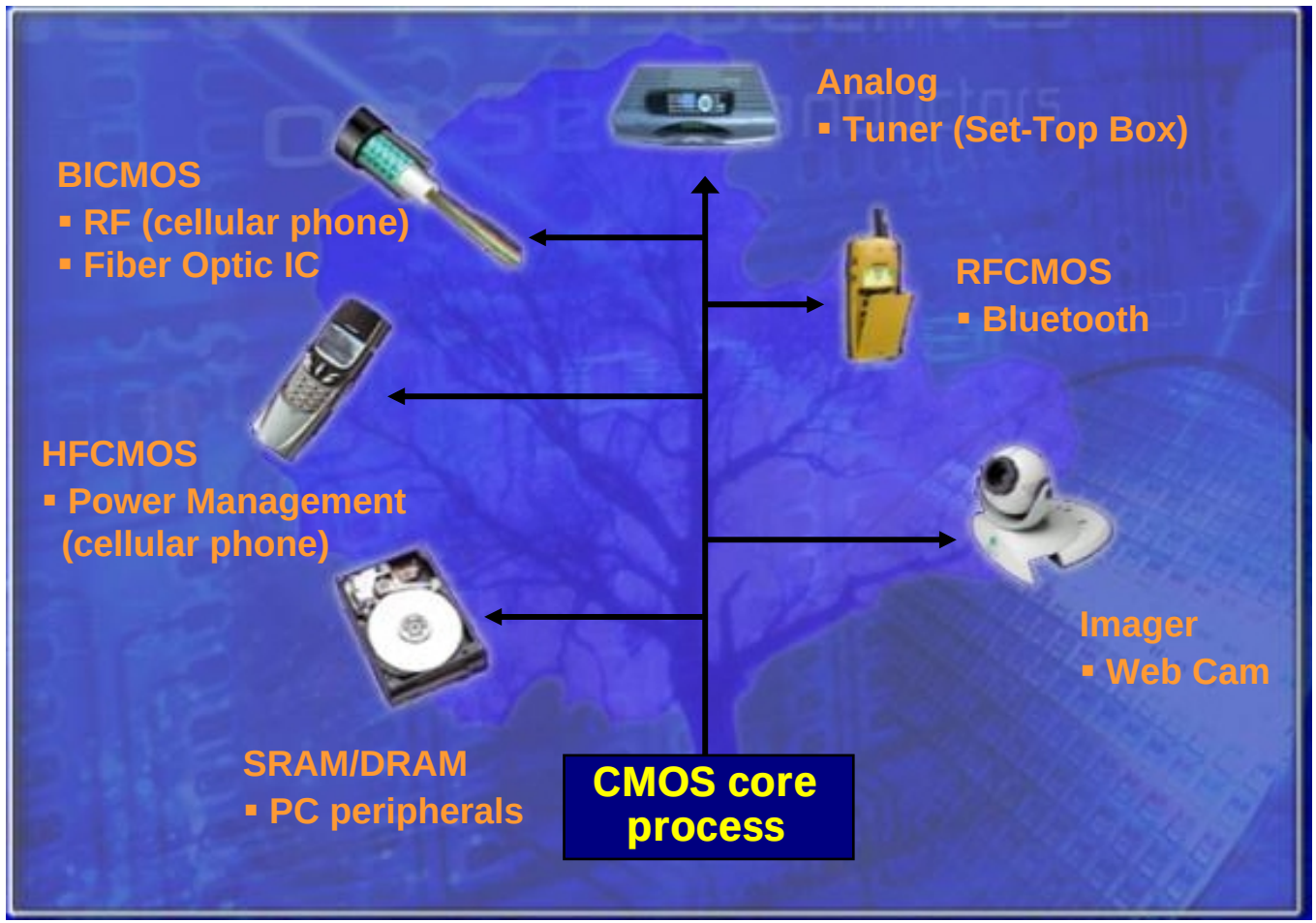


From HCMOS5 (1992) to CMOS065 (2002)

CMOS090 300mm 6LM integration

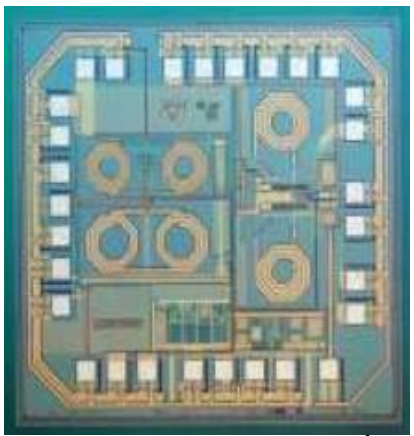


Extending Core CMOS for SOC

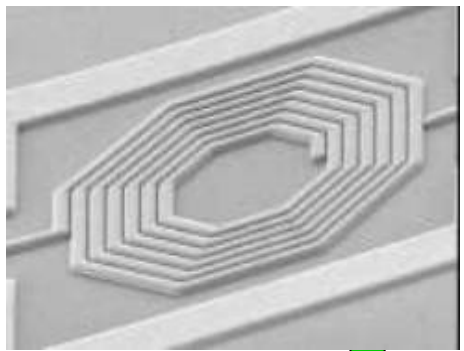


ABOVE IC INTEGRATION

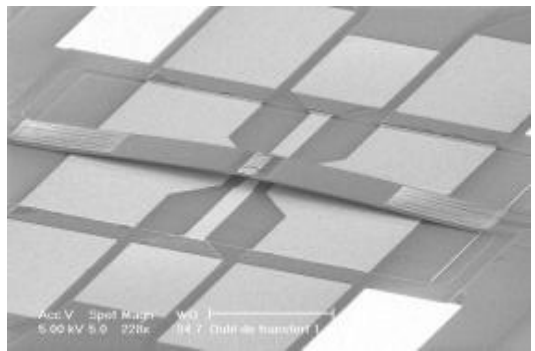
- System on Chip (SOC) approach
- Open the door for innovative architecture & RF front-end



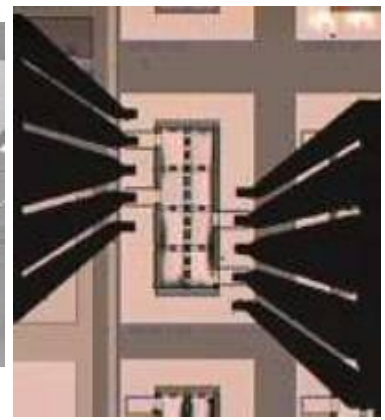
RFIC circuit



High Q inductor



RF Micro-switch

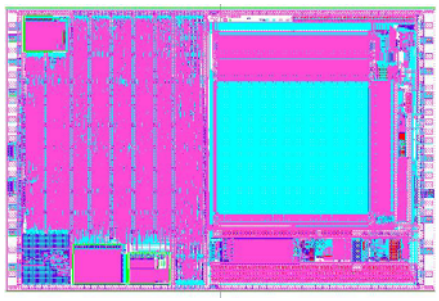


FBAR filter

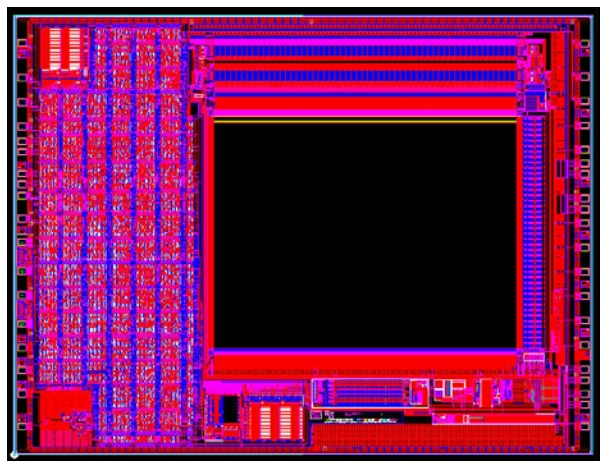
Co-integration of ICs, passives and RFMEMS
New RF functions through strong co-development
between technology & RF design

SoC's with CMOS-Imager process

- **For mobile phone applications:**
  - ✓ **ZS450**: CIF format (~100000 pixels) ✓ **ZS550**: VGA format (~300000 pixels)

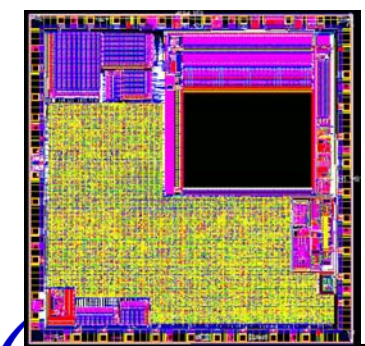


Area
24.0 mm²



Area
39.6 mm²

- **For webcam applications:**
  - ✓ **ZS422**: QVGA format (~75000 pixels)
    => audio/video/video processing (SOC)

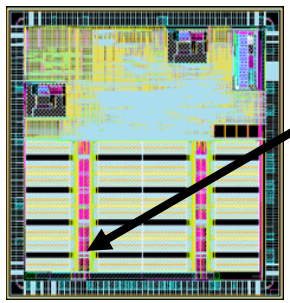


Area
24.1 mm²

Production 0.18um SoC's with eDRAM

Low-End Printer

(20mm²)

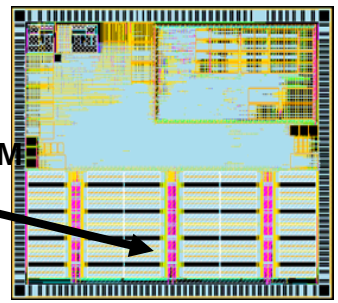


4 Mbits eDRAM

Includes ARM micro

High-End Printer

(34 mm²)



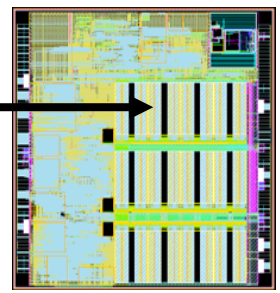
6 Mbits eDRAM

Includes ARM micro

Camera for cell phone

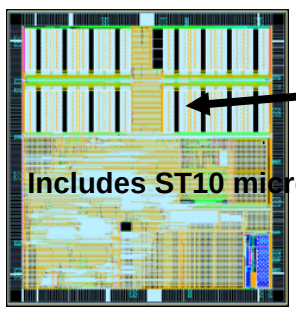
(15 mm²)

3 Mbits eDRAM



Disk Controller

(26 mm²)

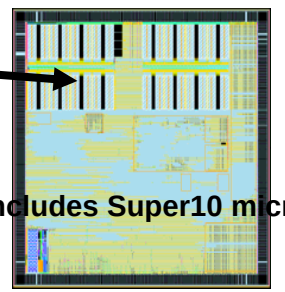


4 Mbits eDRAM

Includes ST10 micro

DVD recorder

(34 mm²)



Includes Super10 micro

Low-Power

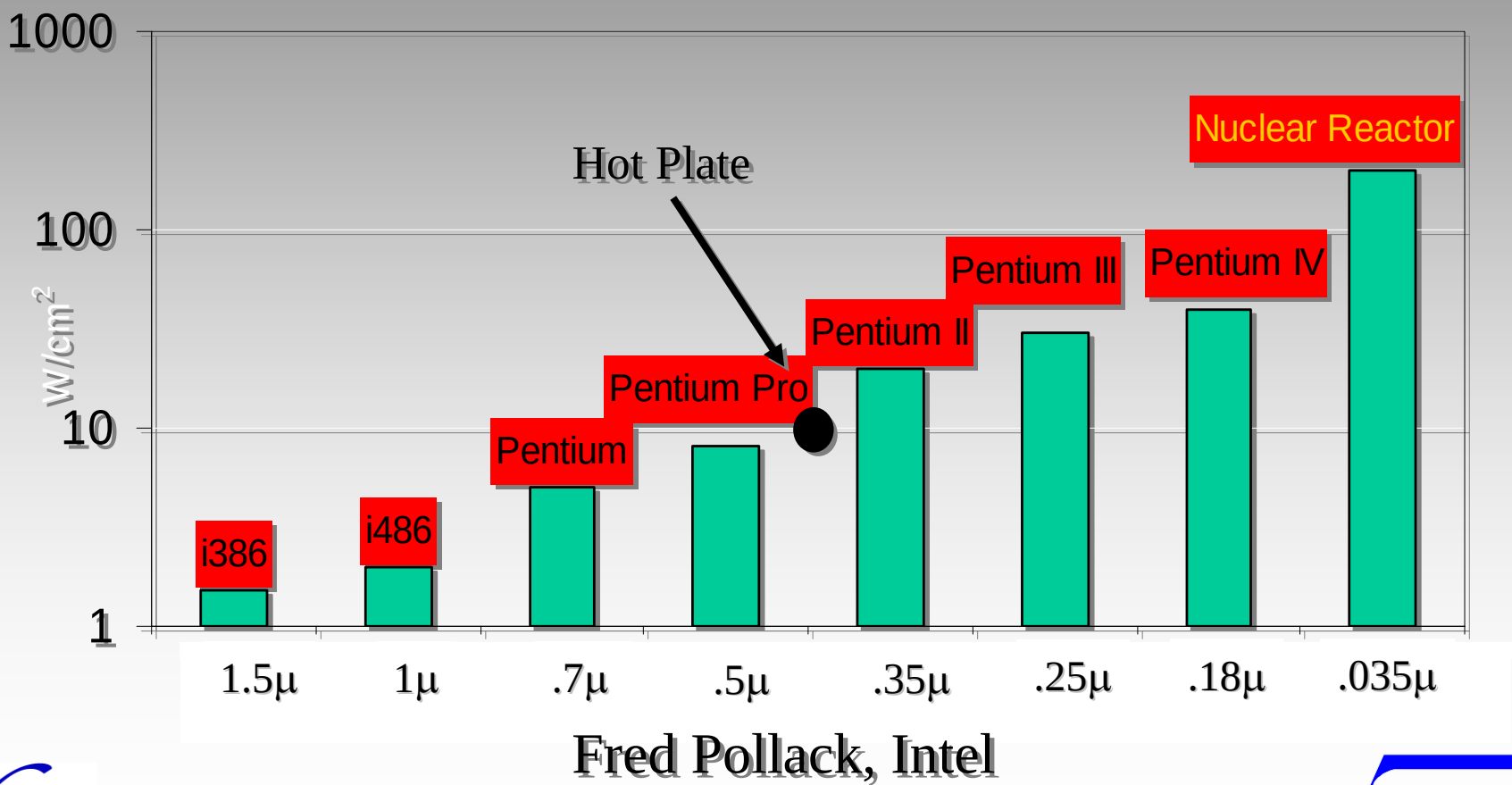
Process / Design Trends

2 opposite requirements for the future

- Increase processing power (GOPS):
  - **Video, Audio, Graphics, Communications:**
    - ✓ **High performance dedicated processors**
    - ✓ **A lot of embedded memories**
  - **Replace Analog by Digital (e.g. digital Radio)**

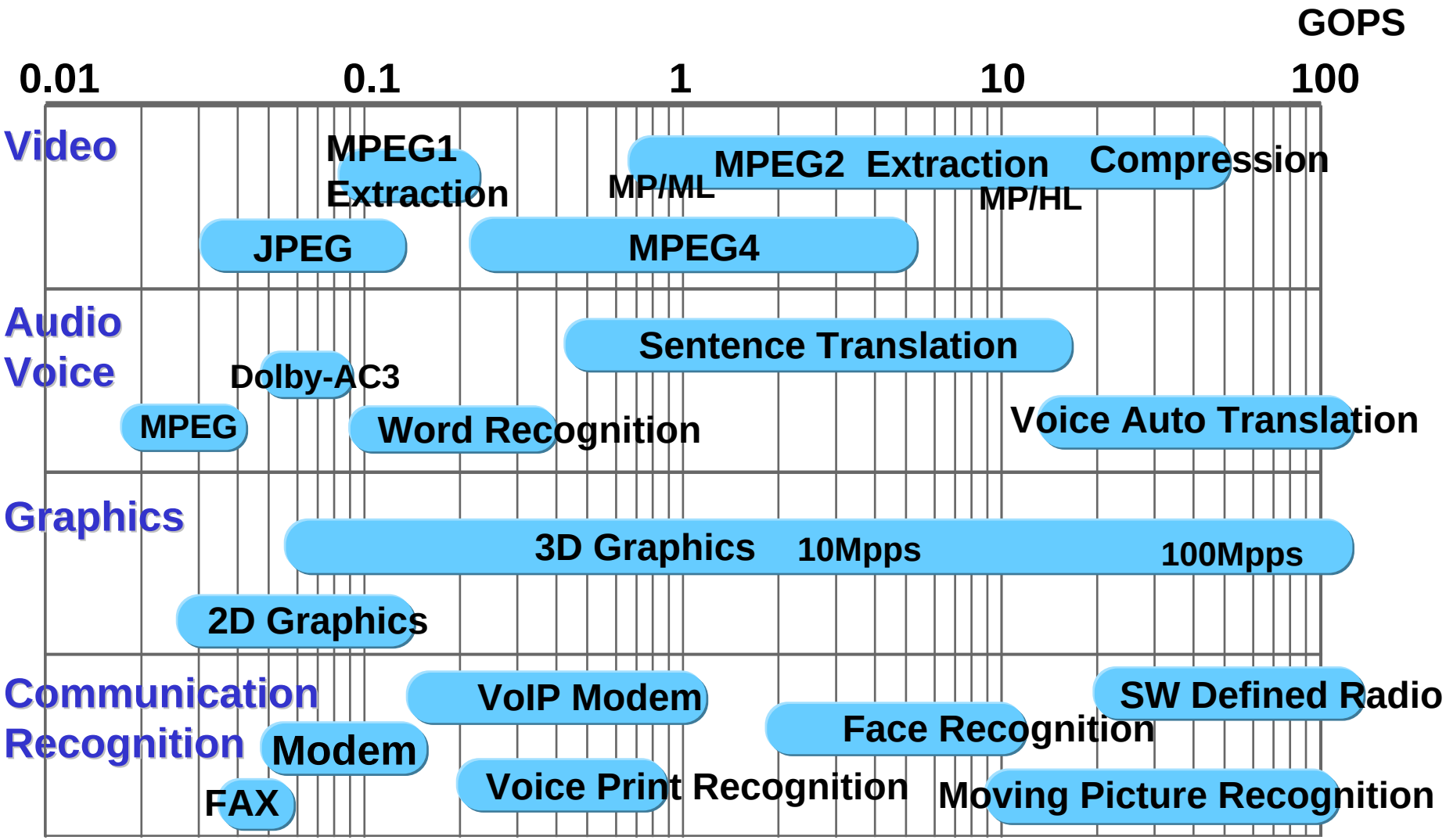
- Reduce power consumption (Watt/Op):
  - **Dynamic power = CV^2f**
    - ✓ **C: Need SOI-like junctions and LowK dielectrics**
    - ✓ **V: decrease VDD to the minimum to achieve Frequency f**
    - ✓ **F: keep Frequency pretty low, use parallelism**
  - **Static power = as low as possible**

Power Density in Microprocessors



Required Performance for Multi-Media Processing

(source ITRS Design ITWG July 2003)



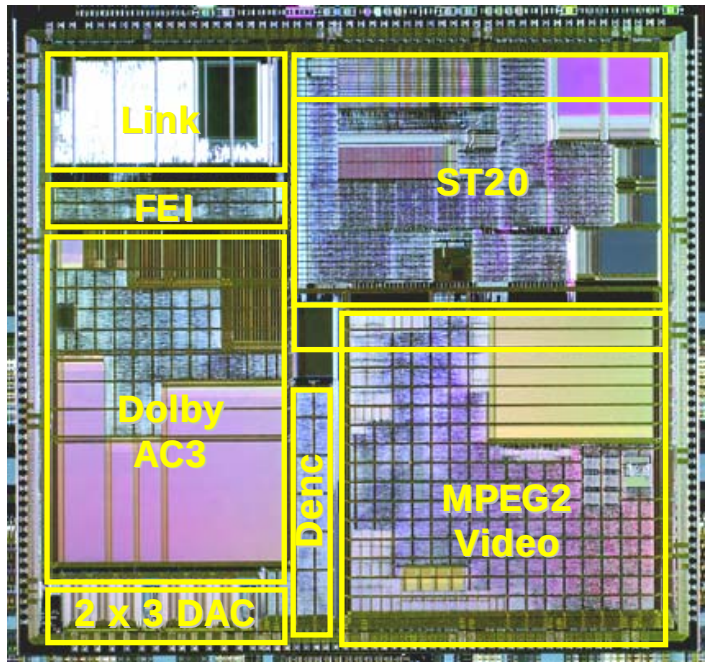
GOPS: Giga Operations Per Second

SoC at the heart of conflicting trends

Time-to-market:

Process roadmap acceleration

Consumerization of electronic devices



Complex systems:

uCs, DSPs HW/SW

SW protocol stacks

RTOS's

Digital/Analog IPs

On-Chip busses

Process options explosion (analog, RF, imagers, …)

Deep sub micron effects:

crosstalk

electro migration

wire delays, on-chip-variation

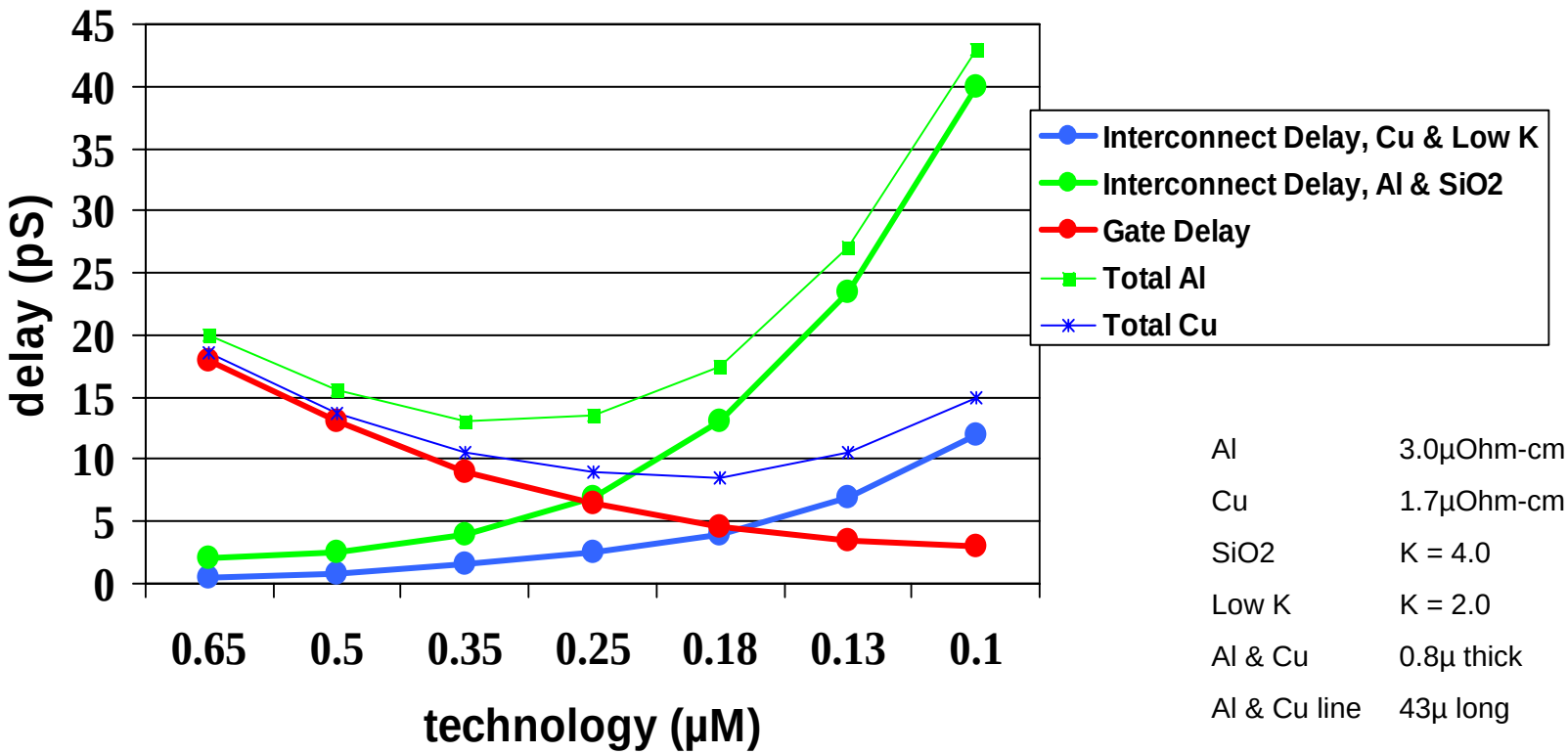
mask costs (OPC, PSM)

copper wires

Static versus Dynamic Power

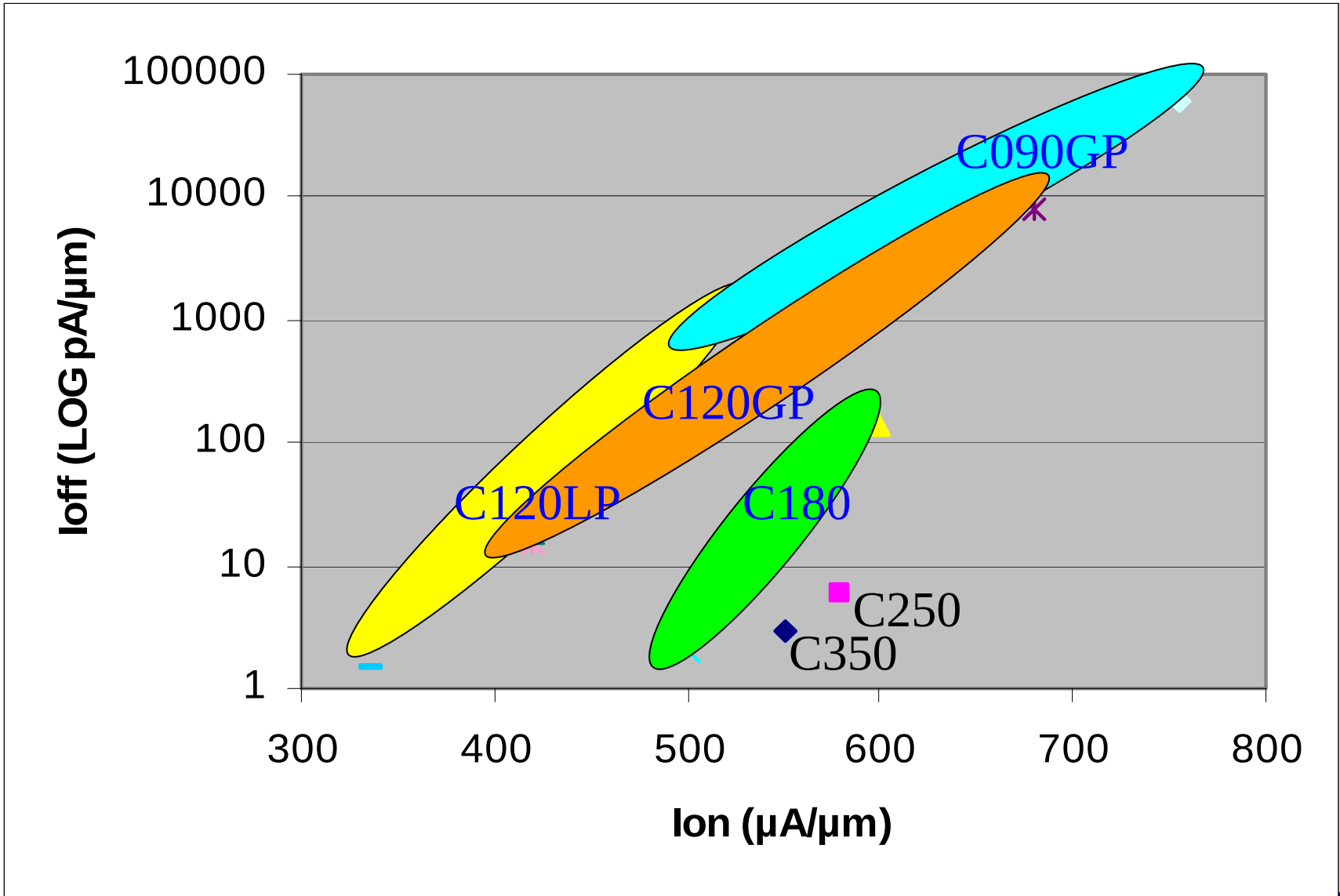
- Dynamic Power per Chip is rather stable due to system limitation: mechanical / battery
- Dynamic Power is under control: $P=CV^2f$
  - VDD is decreasing (slowly)
  - Power management is in practice (clock gating, power shut down, …)
- Static Power is not under control: natural leakage of transistor multiplied by 10 every 2 years:
  - Power shut down is the only way to cut leakage
  - Very low voltage retention or zero leakage Non Volatile memories are potential solutions (Flash, MRAM)
- Static Power is becoming as high as Dynamic Power at high temperature (wasted power, no solution)

Gate and Interconnect Delay vs technology node: Good for Dynamic Power as well



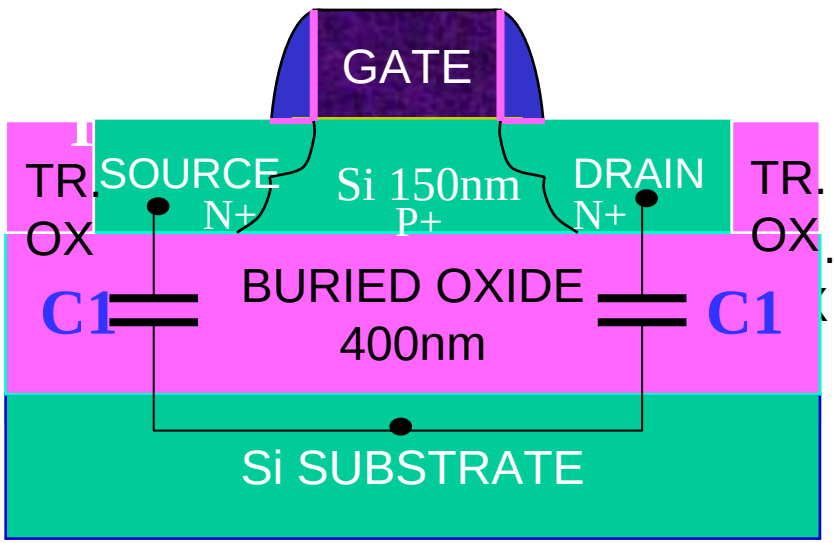
Al	3.0µOhm-cm
Cu	1.7µOhm-cm
SiO2	K = 4.0
Low K	K = 2.0
Al & Cu	0.8µ thick
Al & Cu line	43µ long

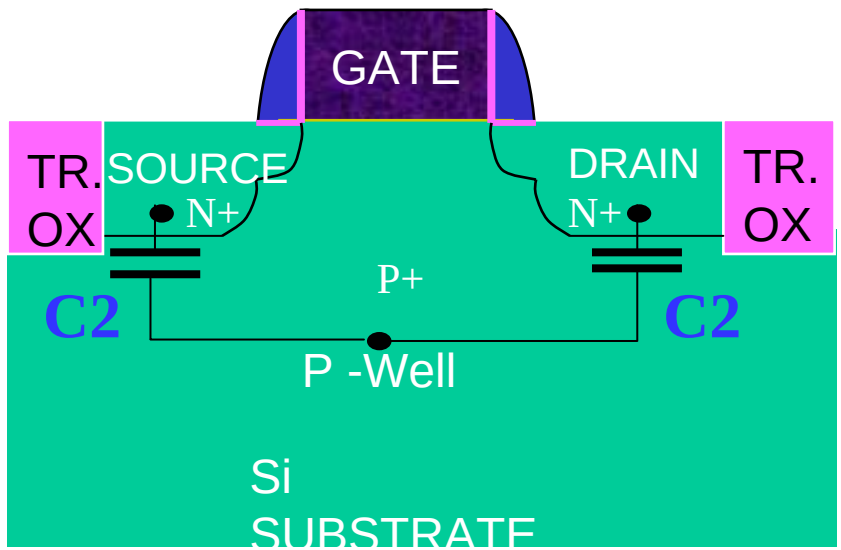
Ion/Ioff evolution is a BIG concern



SOI ?

- **Advantages:**
  - **Reduced S/D junction capacitance**
  - **Full dielectric isolation => latch up immunity**
  - **BOX & STI cap are nearly null**
- **Benefits:**
  - **power/performance improvement**





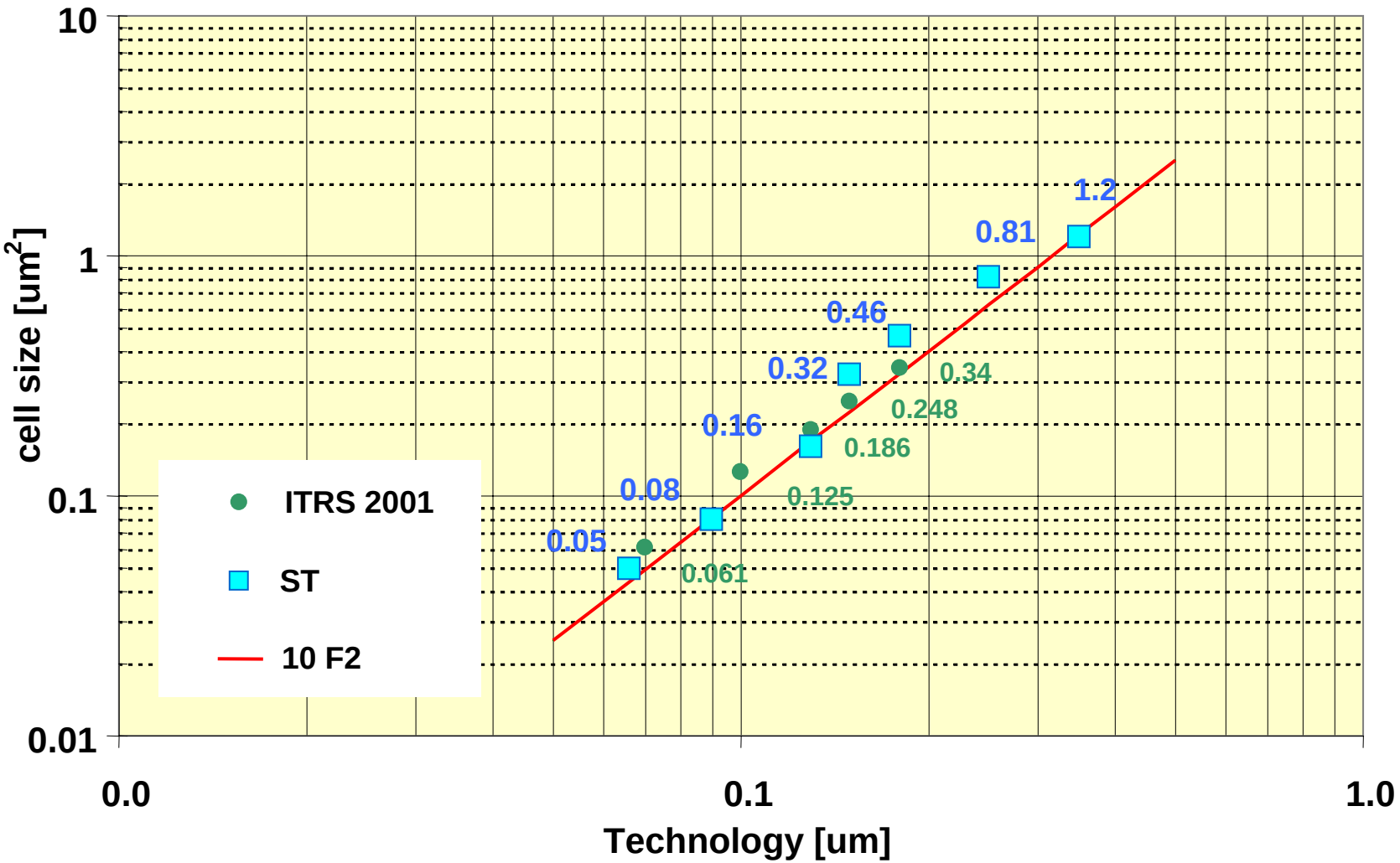
Results in 120nm SOI

- improved performances (on SRAM)

Power Supply	Speed Gain	Dyn Power Gain	Leakage Gain
1.08V	0 %	20%	x 0.1
1.2 V	10%	17%	X 0.15I
1.32 V	20%	14%	x 0.5

- The gain achieved on 0.12um SOI technology corresponds to the next generation on Bulk = 90nm

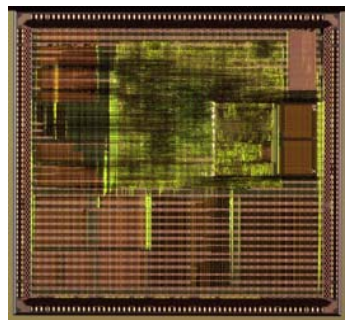
Flash NOR Cell – ST vs. ITRS Roadmap



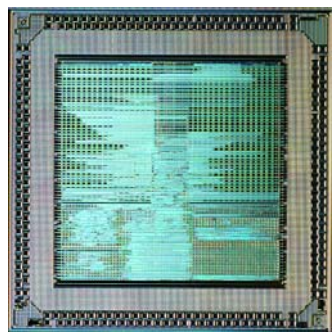
Low Power Design Activities

- System Level
  - RTOS
  - Memory size and bandwidth optimisation
  - Architecture Power/Performance trade-off
- RTL to Layout
  - Activity control
    - ✓Gated clock
    - ✓Power based synthesis
  - Leakage control
    - ✓Supply control
    - ✓VT control thru back-bias
    - ✓Mix High-Speed and Low-Leakage
- Smart Power/Low-voltage operation
  - ✓Multi-voltage support
  - ✓On-chip voltage regulator(s)

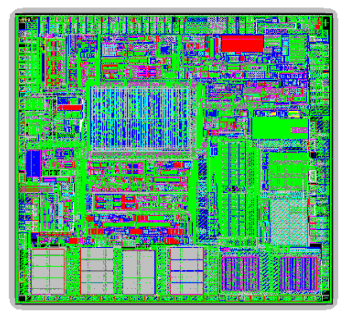
Research activities
Labs / Universities



Disk Drive Controller
0.13um

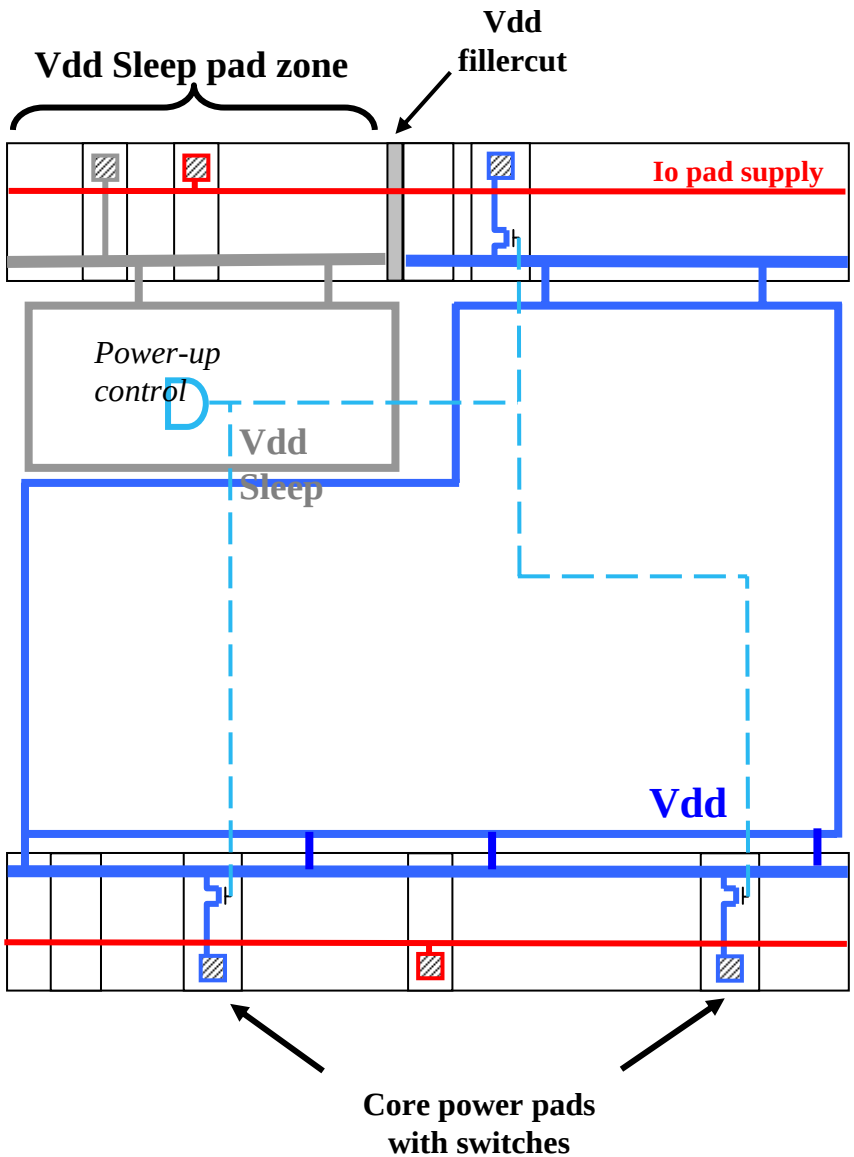


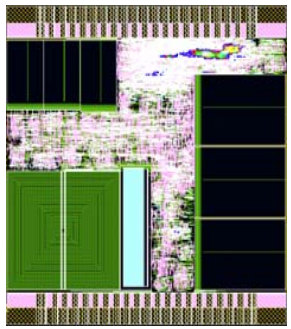
90nm ST20 / ST40



0.25um
SiGe BiCMOS
GSM Power Management

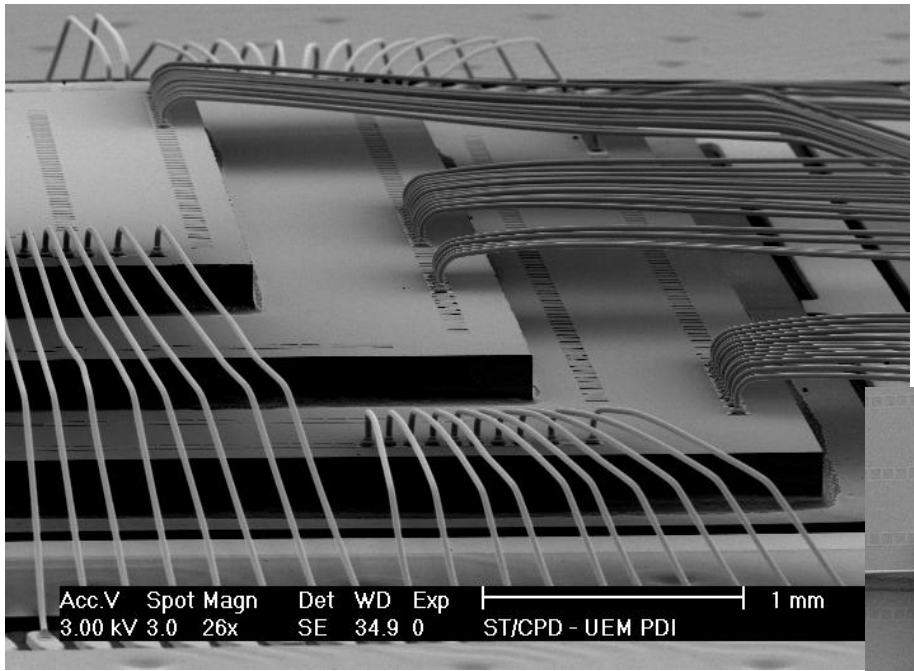
Low-Power techniques for wireless





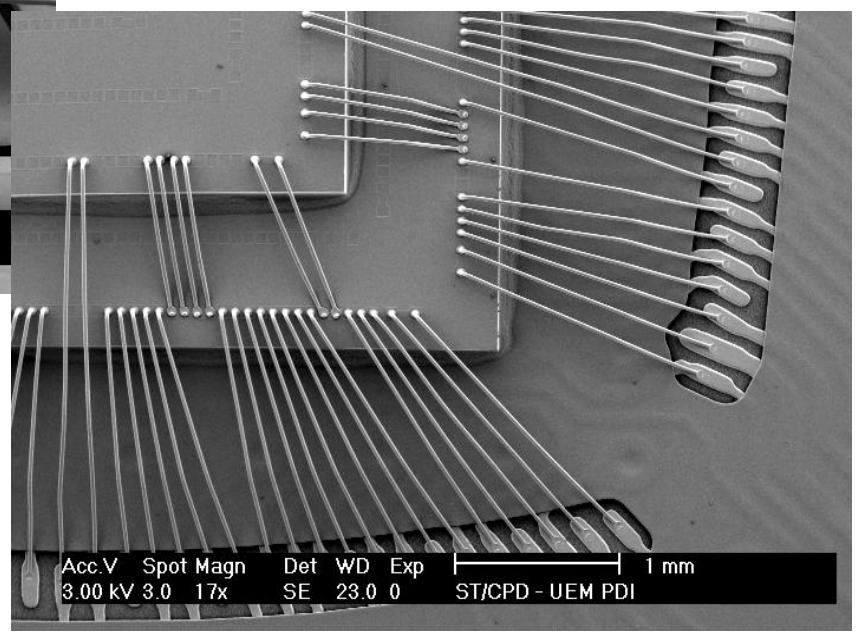
- Two supply zones: Vdd and VddSleep.
- Specific rules at RTL for boundary between Vdd and VddSleep areas
- Gnd is common for all cells.
- Pads are always powered.
- 3 power pads with embedded switches

Single Package Triple Stacking



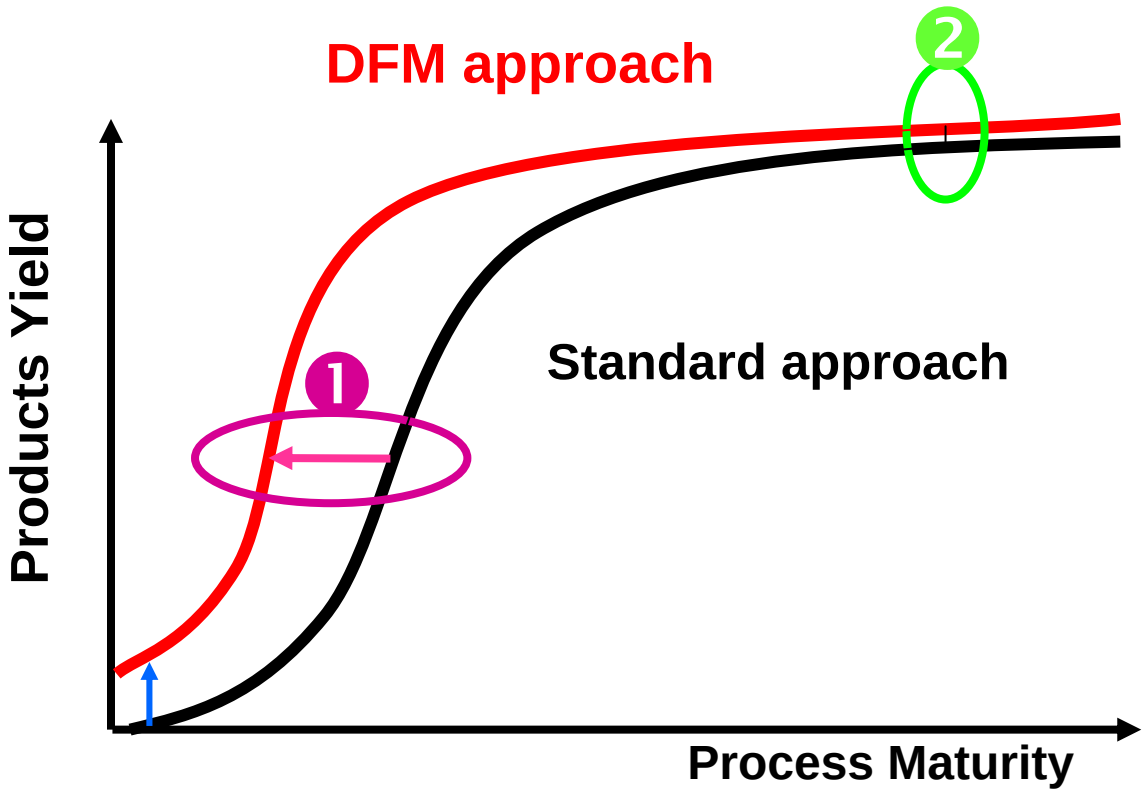
Triple stacked die

Multichip chip wire bonding



Design / Manufacturing links

Design For Manufacturability Gains



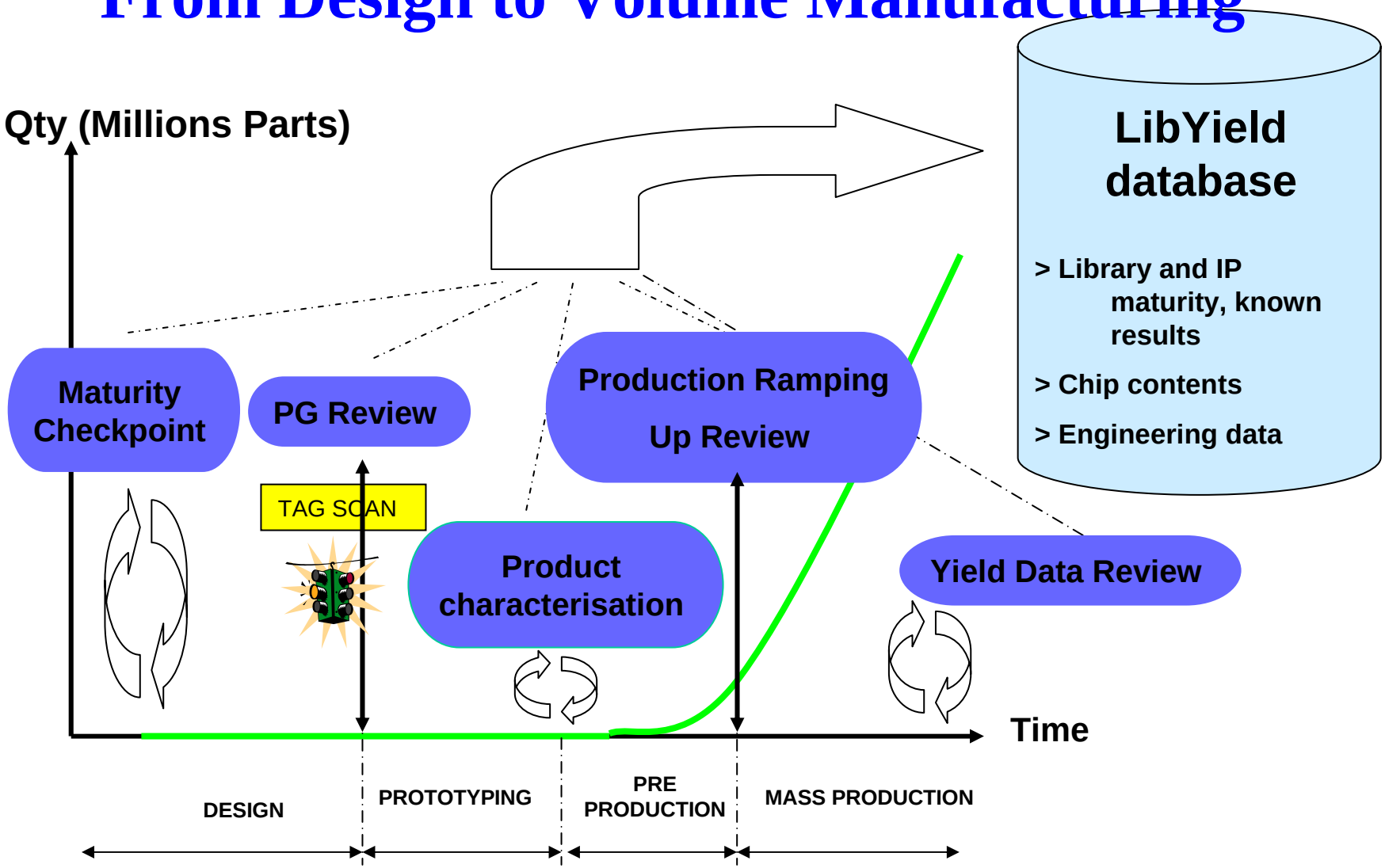
1 **Acceleration** for **ramp-up** process (~months)

2 Yield gain for **mature** process (3 to 5%)

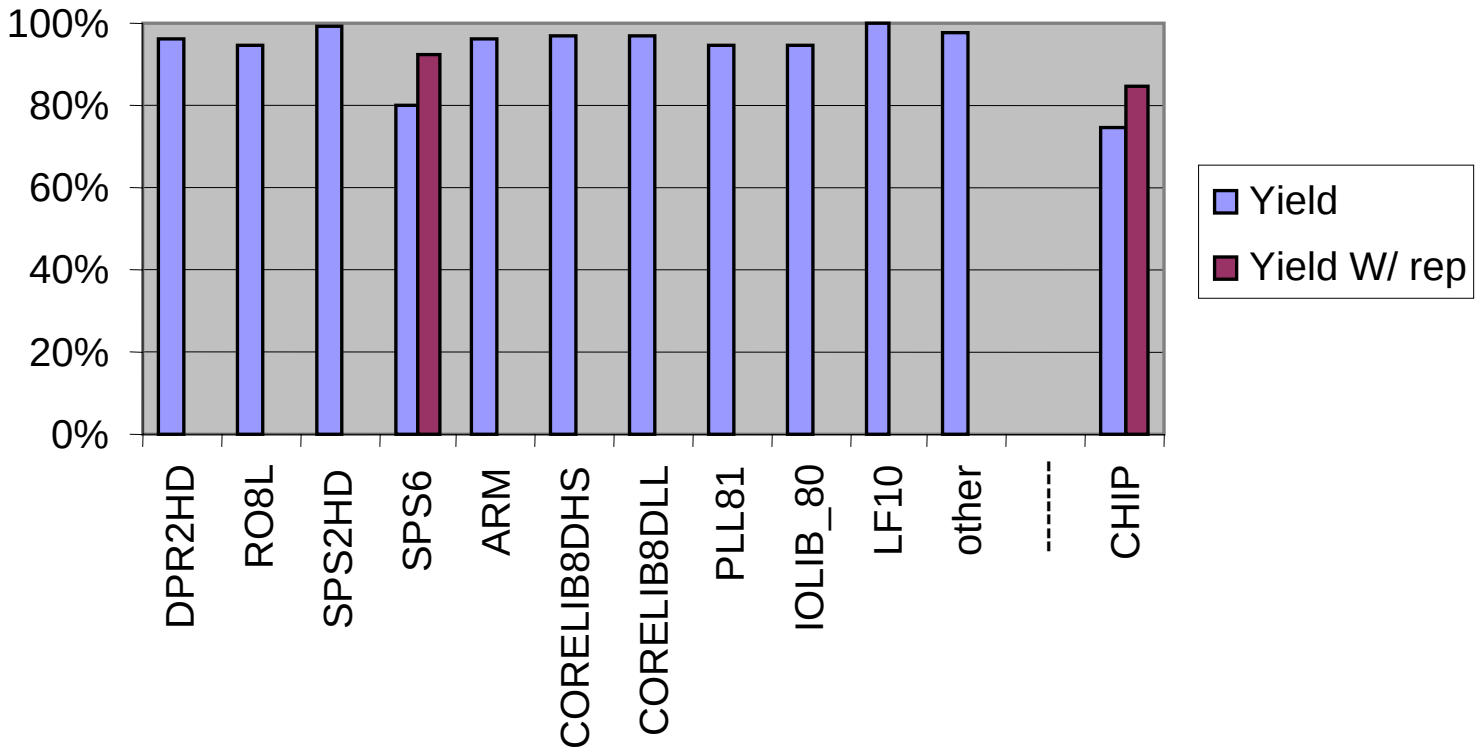
3 Robustness increase (versus design marginalities)

4 Reliability improvement

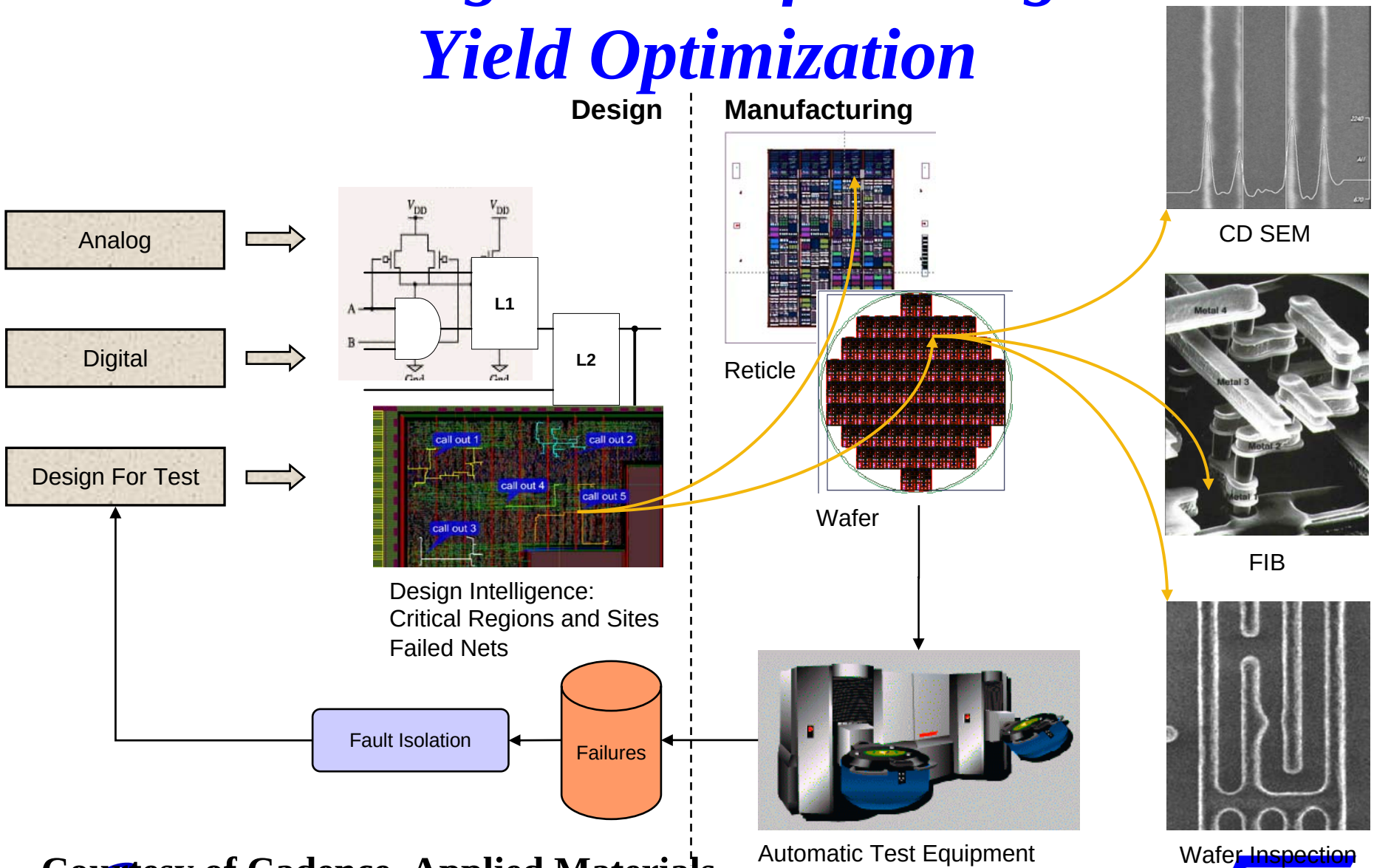
Impact of Test: From Design to Volume Manufacturing



Predictive Chip Yield based on IP content



Design / Manufacturing Yield Optimization



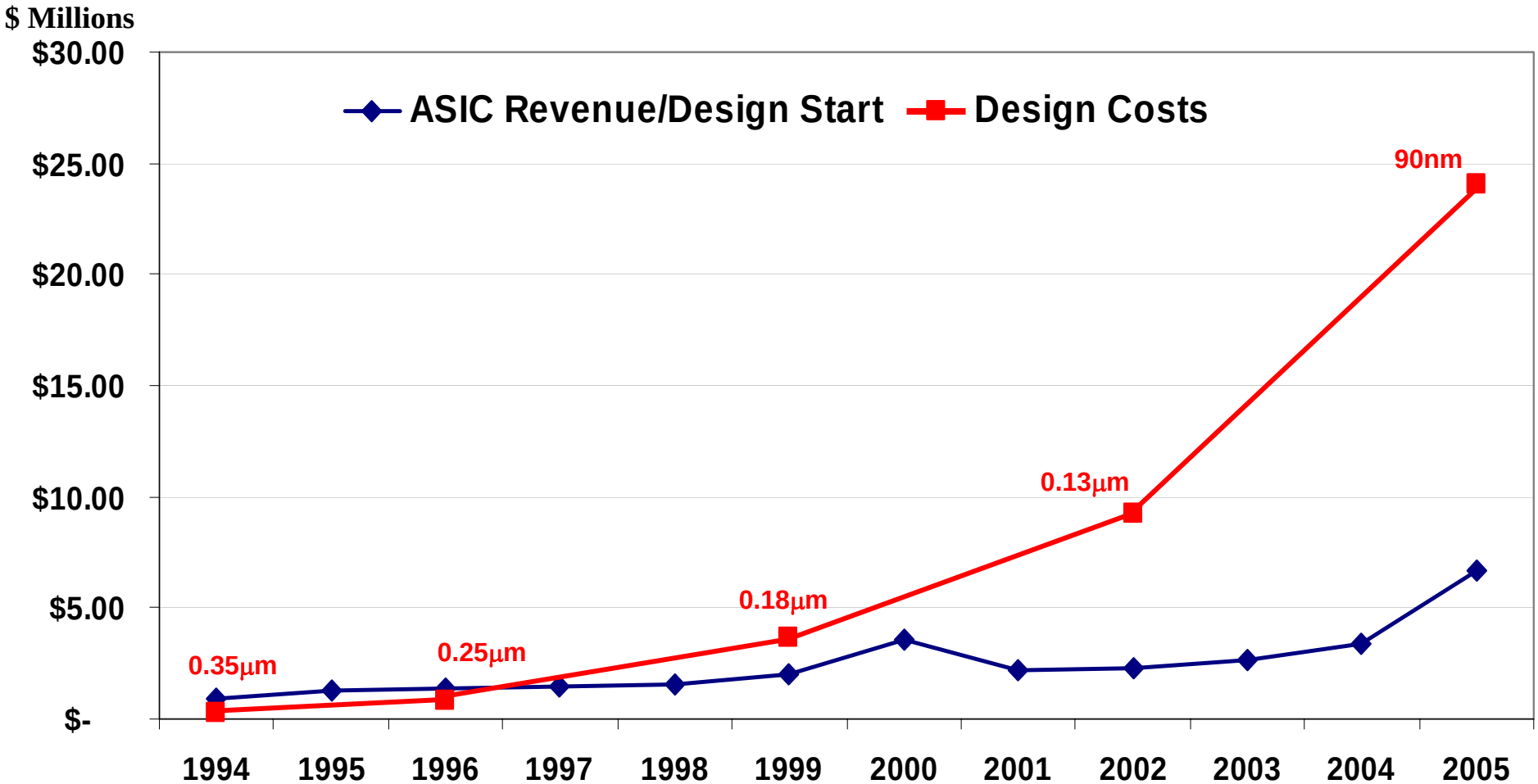
Courtesy of Cadence, Applied Materials

SOC design challenge

Today's Reality

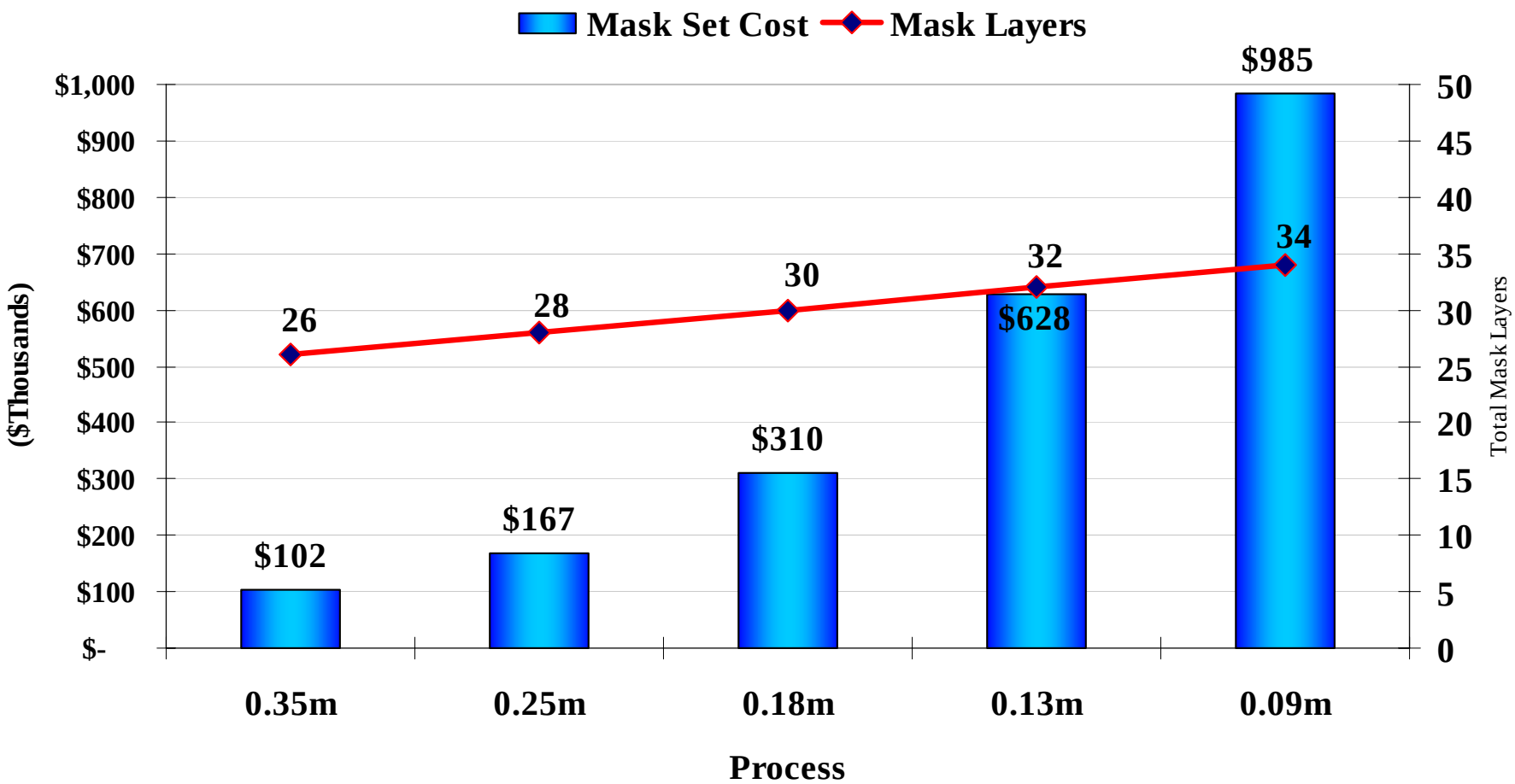
- Complex SoC projects are draining the companies resources and developments are lagging behind the technology capacity.
- Today SoC project non-recurring expenses (NRE) are 10-50M$ should have 50-500M$ revenues to balance an acceptable ROI.
- Several $B already invested on IPs and integrated functions during last years.
- Design re-use must be exploited at all levels included sub-system re-use.

Revenue per ASIC is Not Increasing as Fast as Fixed Costs of Cutting Edge Design



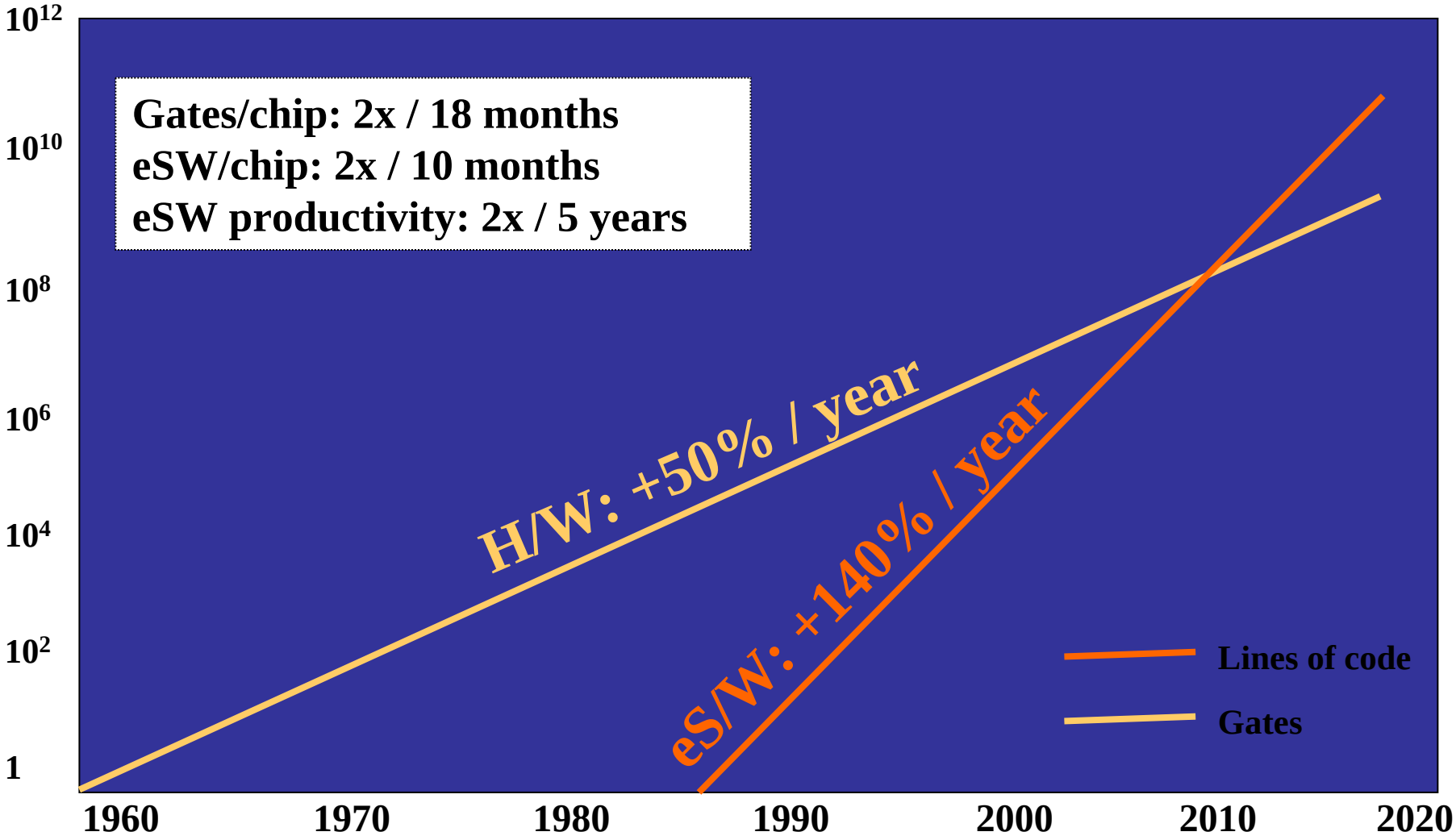
Source: Gartner Dataquest 2002/2003; I.B.S. 2002…Custom EDAC Study

Photomask Costs Are Increasing…

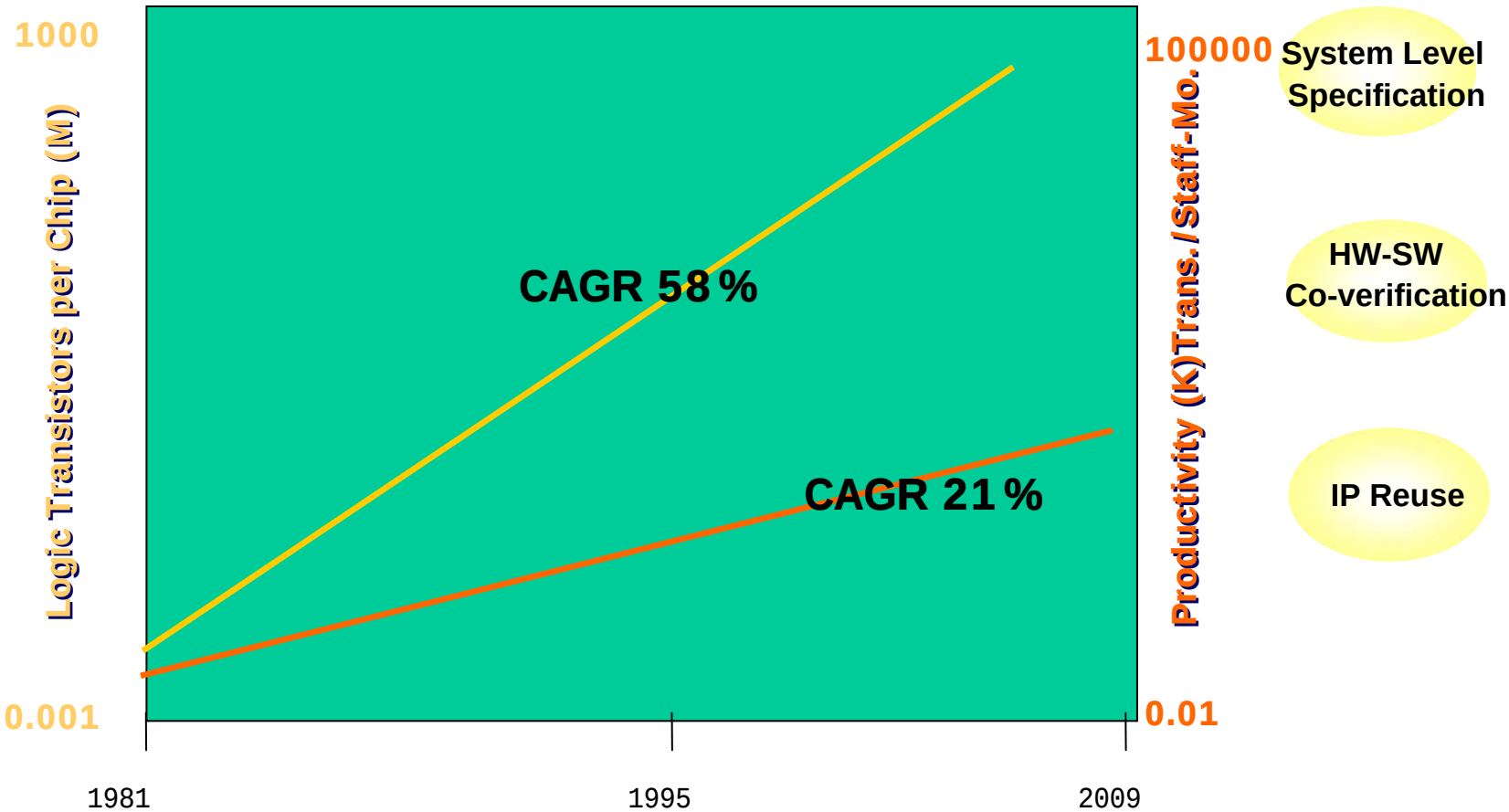


Source: IC Insights, 1/2003

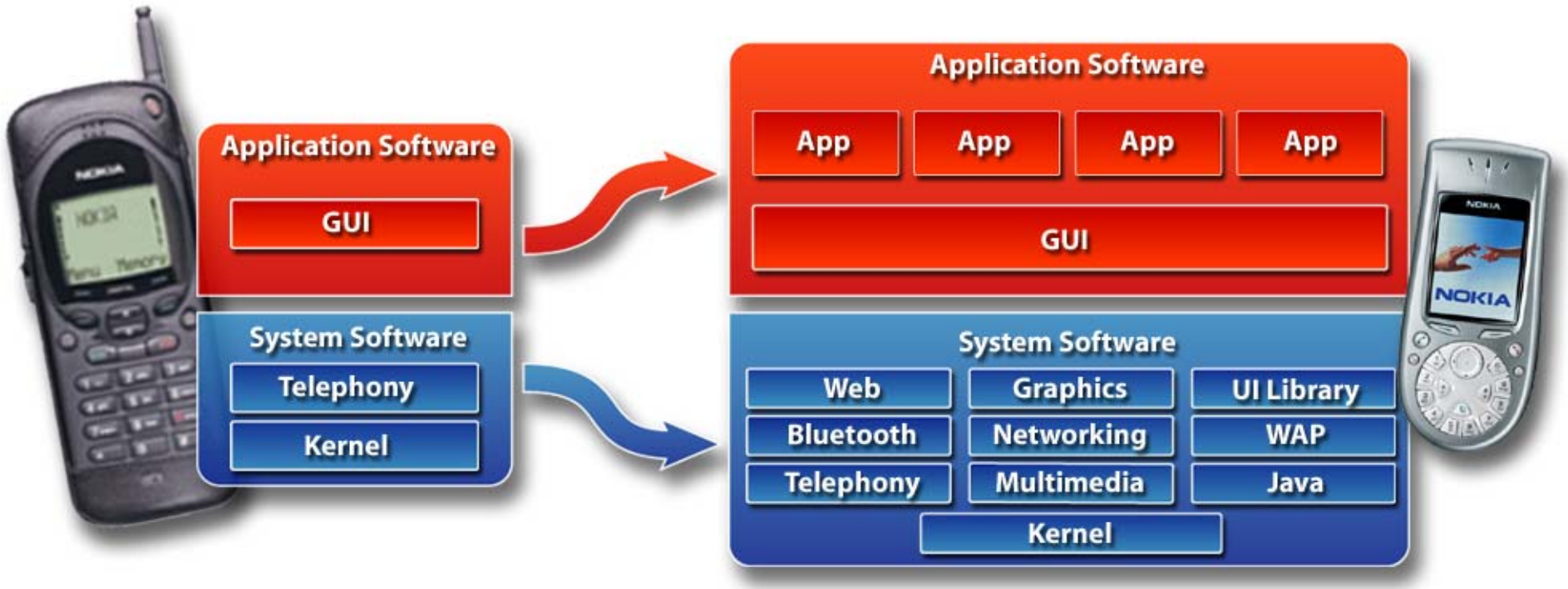
S/W and H/W Complexity Factors



Closing the Design Productivity Gap

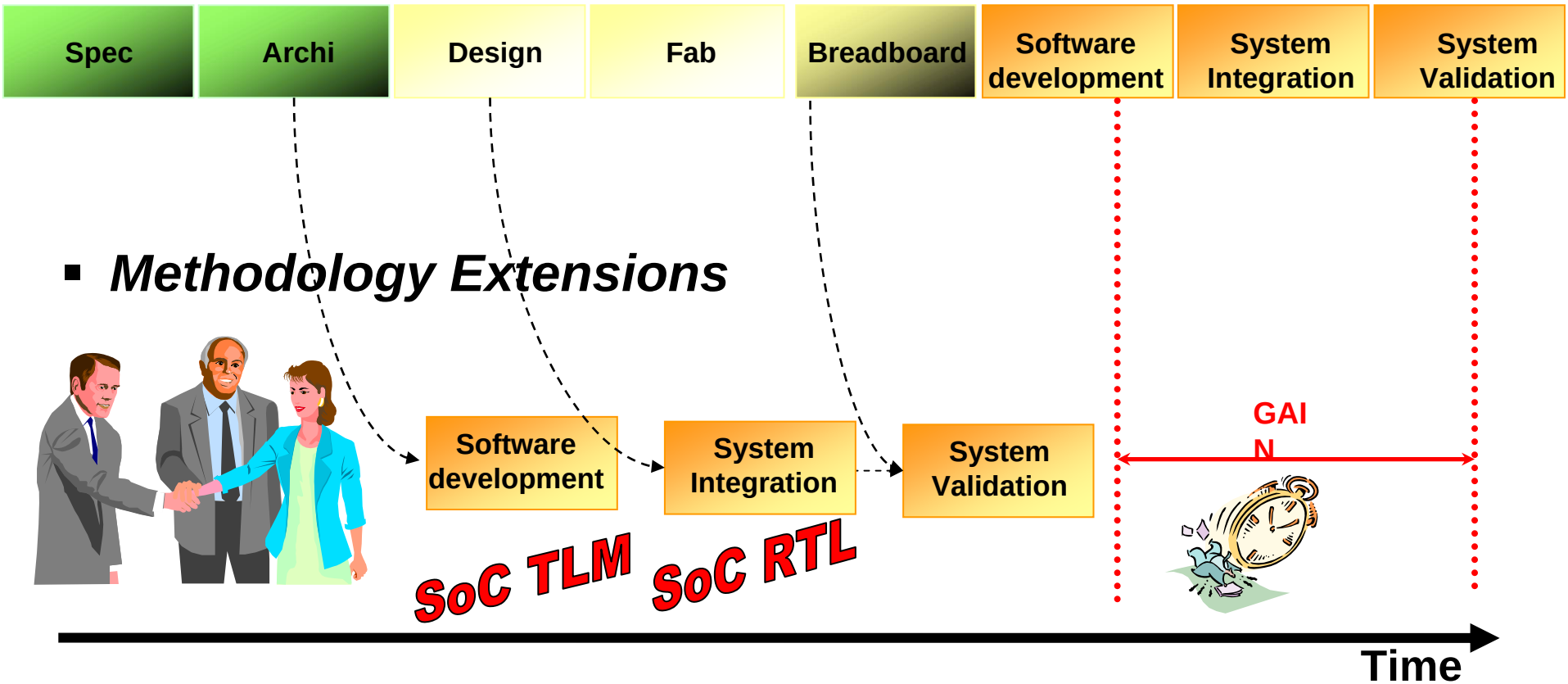


Embedded Software Development Requires as Much/More Design Effort Than Hardware



Concurrent Hardware/Software Design

- ***Standard Flow***



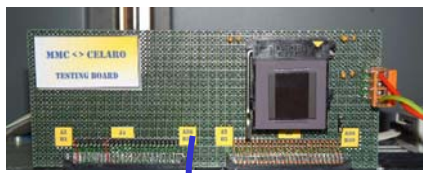
- ***Methodology Extensions***

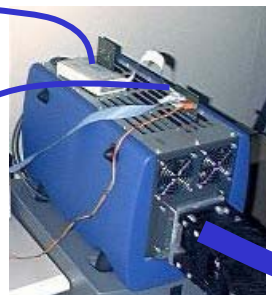
HW/SW fast prototype platform

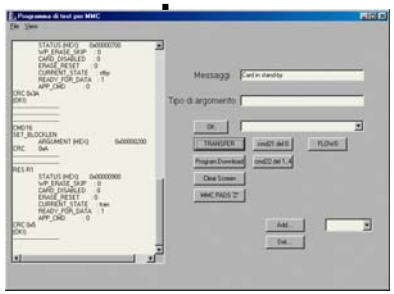
- Faithful representation of the final design
- Available much sooner than the final silicon
- Guaranties the real-time behavior
- Validation of the fundamentals of the SoC HW/SW architecture

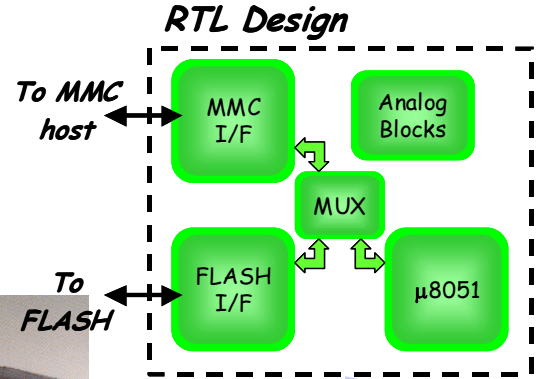
HW Emulation

- Real M58LW128 FLASH chip in-circuit



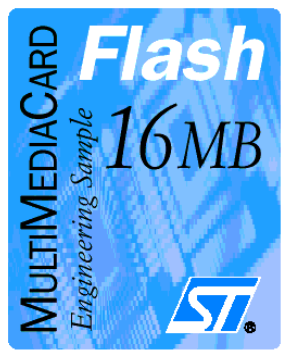




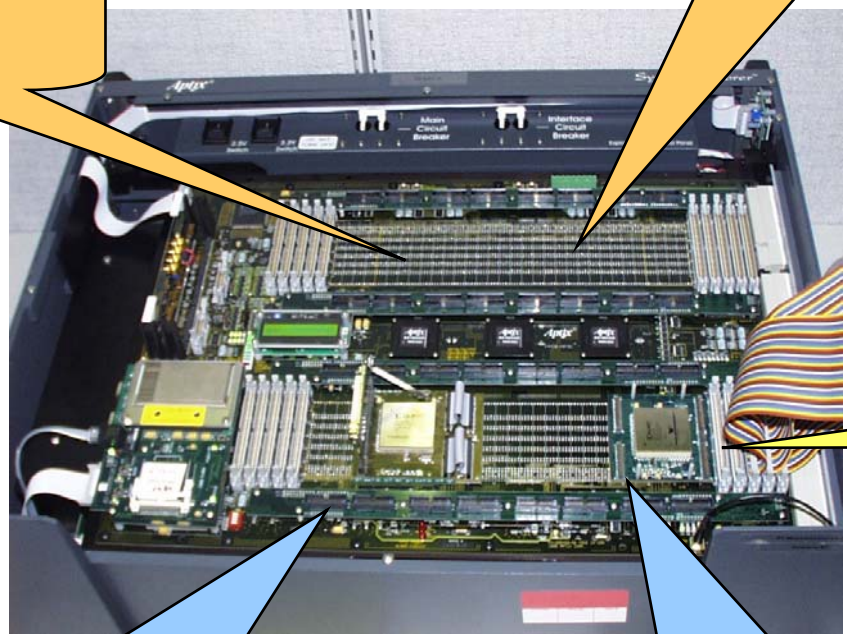


- 1w setup-time
- ~0.5MHz

- SW host running @100KHz
- Connection of HW host ongoing



First Prototype Platform: Aptix



ARM7 Module

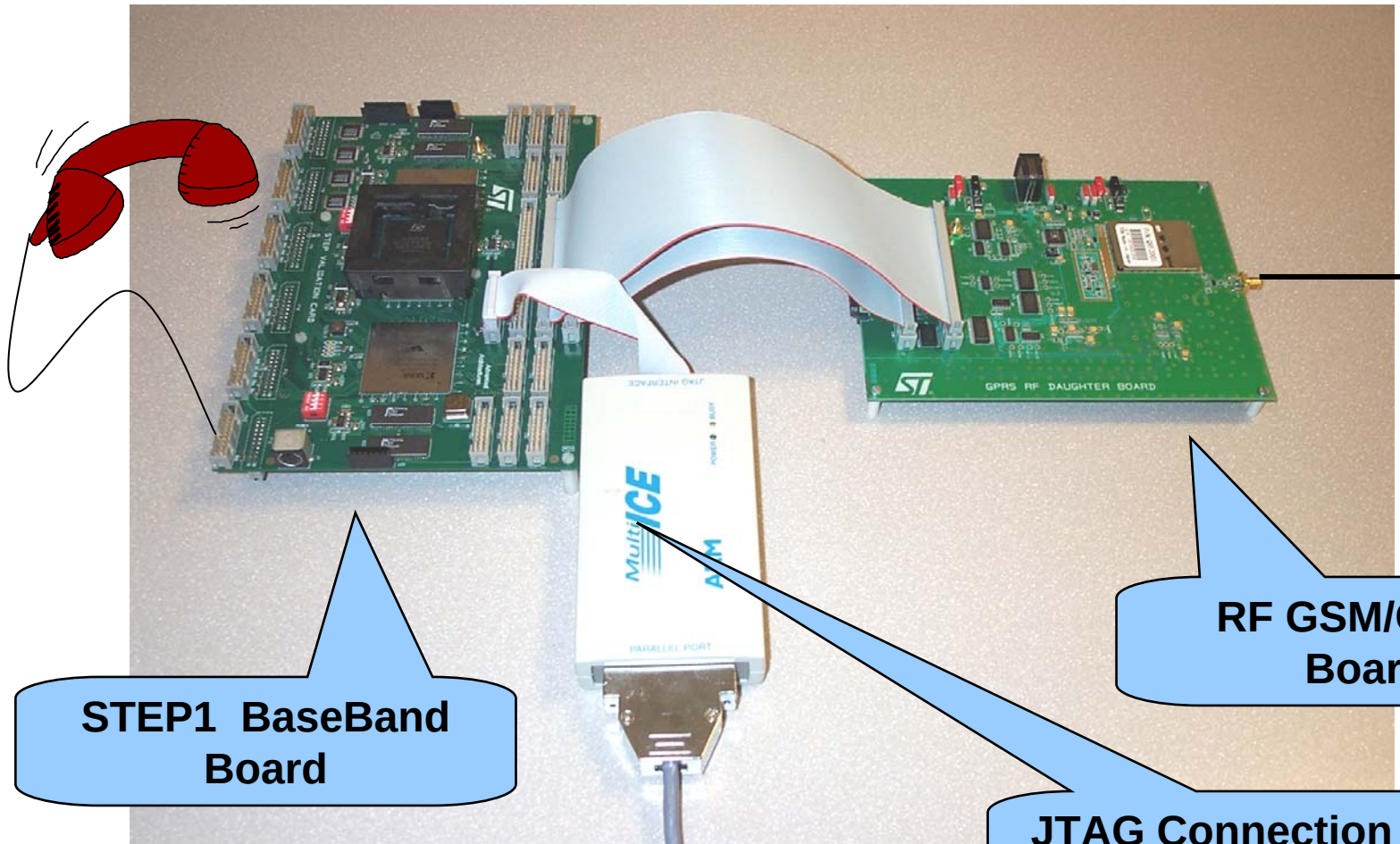
ST120 Module

Interface to RF/Tester

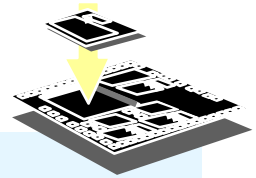
Virtex FPGA (GSM/GPRS modem)

Memory boards

FPGA-based Prototyping Environment

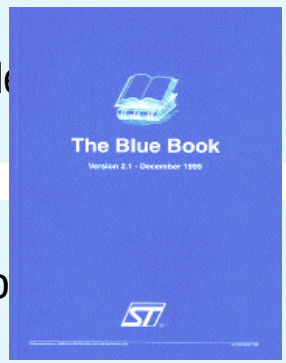


IP Reuse Program

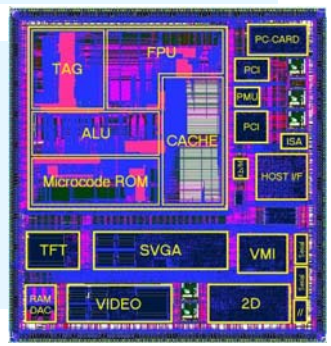


- Organization
  - company program — "Design Methodology & IP Reuse", CEO sponsored
  - corporate driven — CR&D + cross-divisional Committee
  - domain-specific Work Groups — RTL2Layout, AMS, SLD, DFT, Functional Verif., Power, ...
  - intranet information site — CAD On Line portal > K9 IP Reuse Pages

- Reuse standards
  - adherence to industry approach — VSIA; RMM; Quality
  - deliverables / views — **BlueBook** + Unicad Extension
  - IP packaging — bbview (mapping from BB logic views to IP physical files)
  - HDL coding style — **Design Conventions** + HAL associated checking tool
  - On Chip Bus — VCI-close STBus; AMBA



- Methodology
  - Development flo — Synopsys based **Quartet**
  - OCB support — STBus, AMBA Platform kits
  - System Level — SL model deliverables (TLM, BCA...)
  - Verification — dynamic, formal, H/W-S/W, integration



- Infrastructure
  - Design Data Manag[t]., Bug tracking — Products from Synchronicity, Rational
  - IP Quality (IP=Product) — **IPScreen** Certification; **LibYield** Maturity tracking
  - IP Procurement — **IP On Line** catalog; Procurement, Exchange procedures

IP certification
USB2.0 example

5 Summary

FS EBCV functional tests
PASS

HS EBCV functio
PASS

Device High-Speed

EL_2 PASS
EL_4 PASS
EL_6 PASS
EL_7 PASS

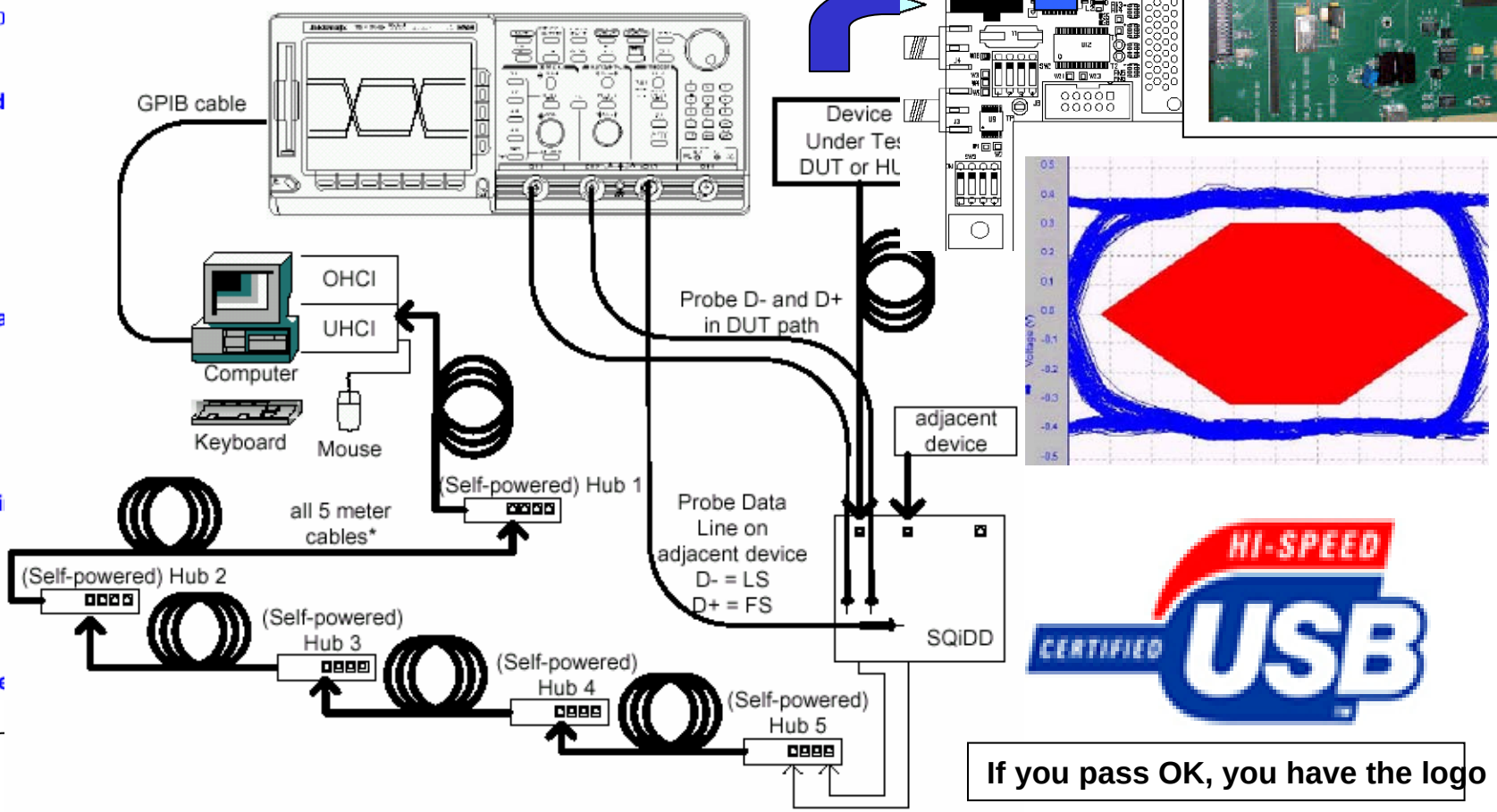
Device Packet Para

EL_21 PASS
EL_22 PASS
EL_25 PASS

Device CHIRP Timi

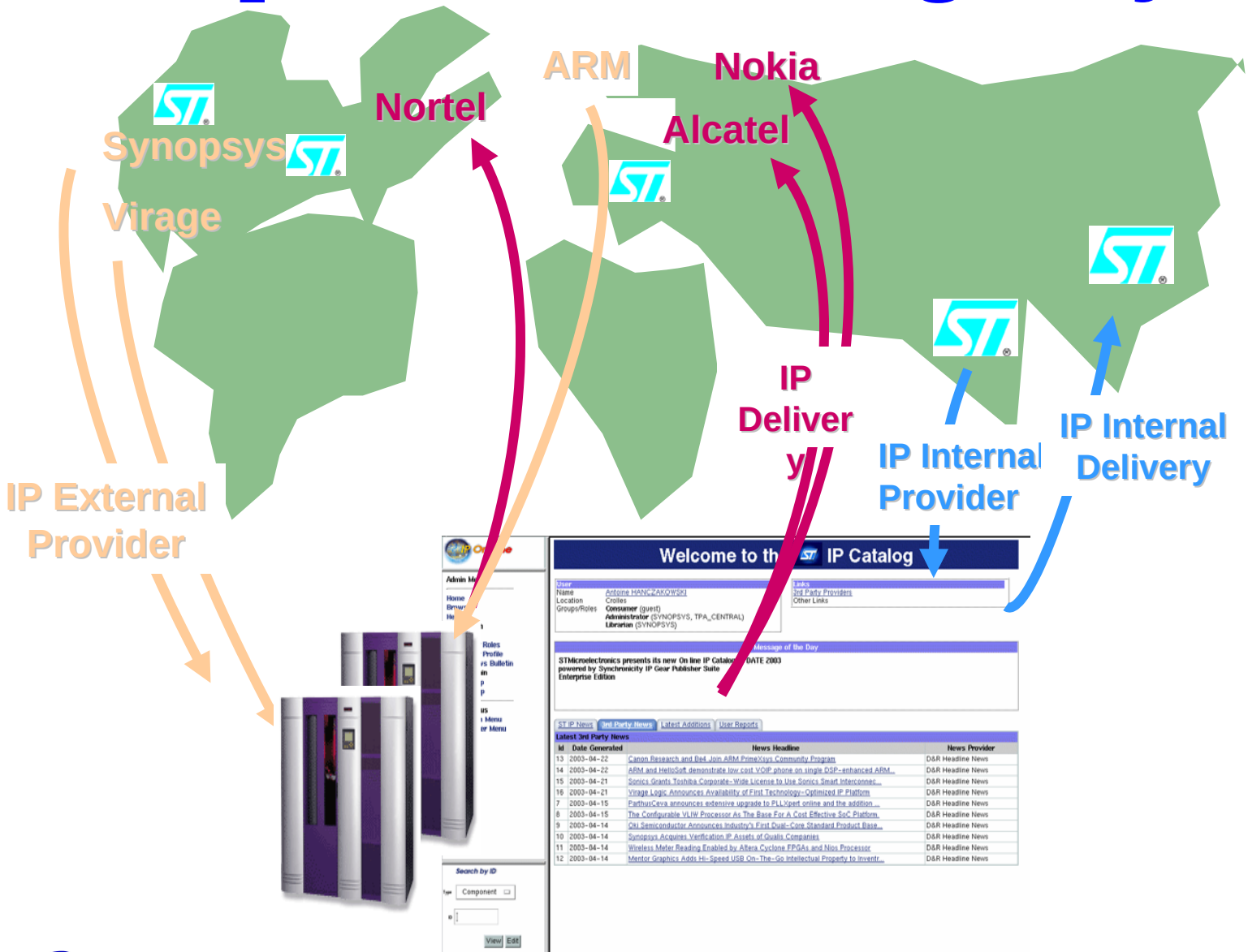
EL_28 PASS
EL_29 PASS
EL_31 PASS

Device Suspend/Re

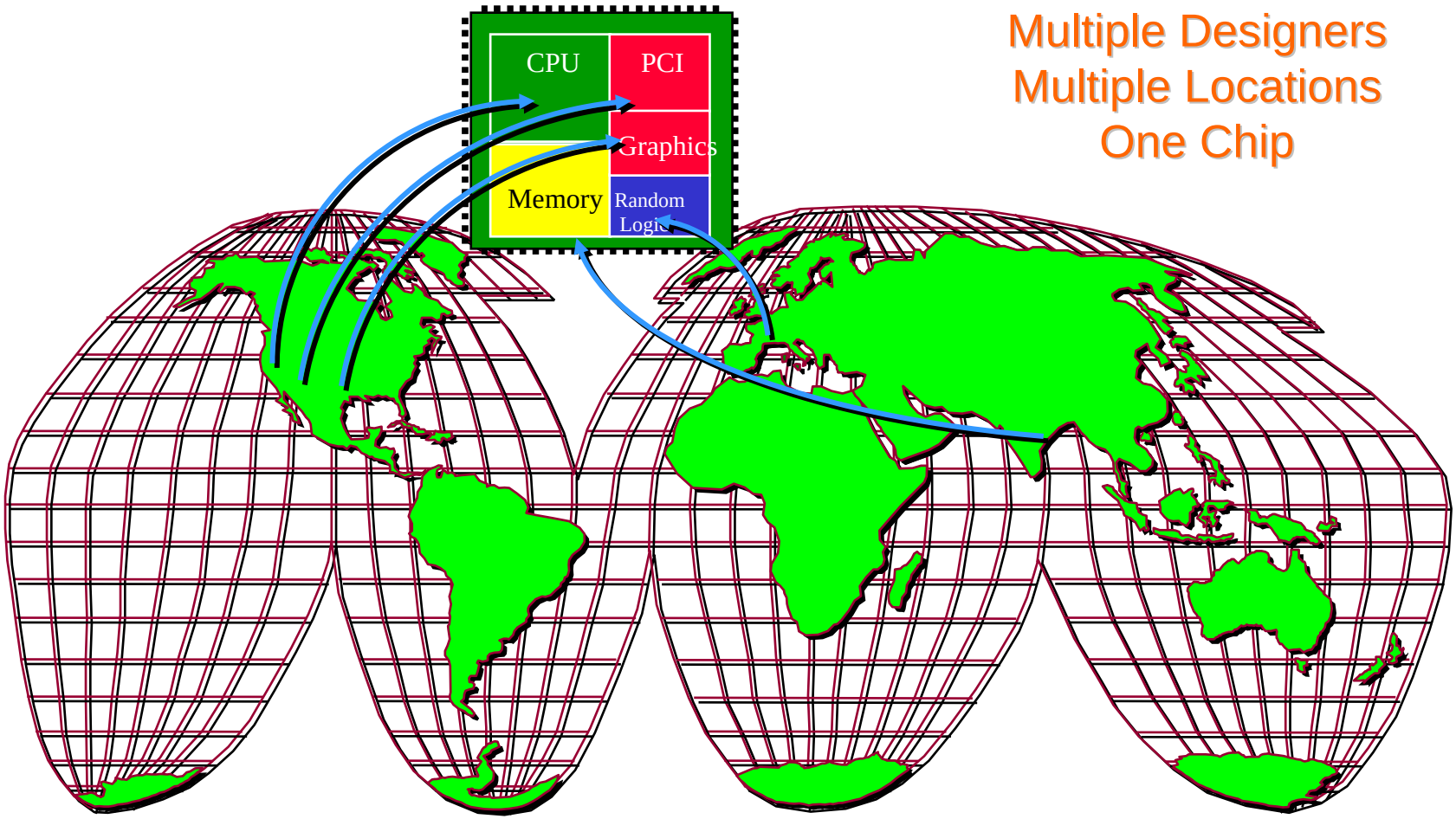


If you pass OK, you have the logo

Corporate IP Catalog Project



Multi-Site Collaborative Design (Synchronicity-based)



Network on Chip

- In 45 nm technologies, the intra-chip propagation delay is predicted between six and ten clock cycles
- Wire issues increase reaching up to 20% of the project design efforts
- **Latency**
  - the intra-chip propagation delay
  - Processor clock cycle times / memory access times
  - Processors / Co-processor
  - Within five years, the large majority of SoCs will run on heterogeneous embedded processors.
    - ✓ Today simple Set-Top Box SoC host 6 different processors
- On-chip traffic management **between integrated functions and the associated** methodology **will be the forthcoming challenges**
- Focus and complexity are moving
  - **FROM GATES TO WIRES**

Flexible and Reconfigurable SoC

SOC flexibility and Configurable Logic

❑ SOC emerging problems

- rising cost of masks
- shorter market windows
- need to quickly adapt to new customer requirements

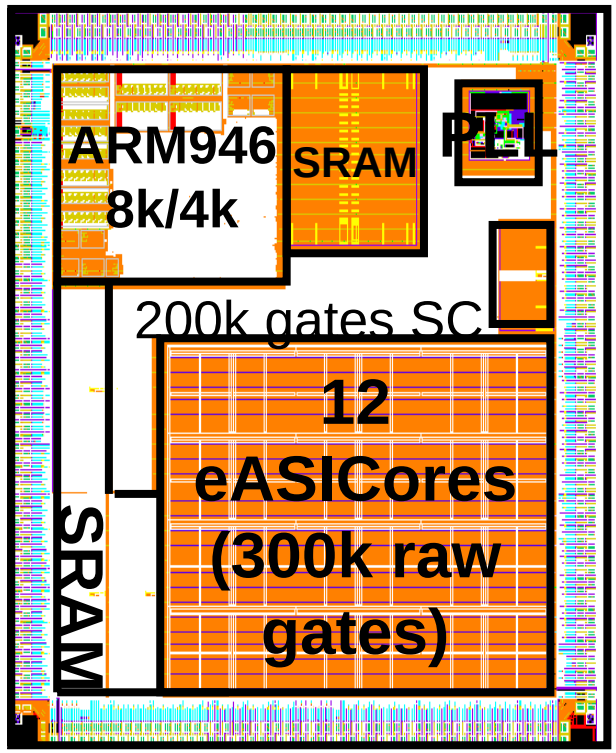
→ need of

- level of programmability
- flexibility on-chip

❑ Set of solutions to be provided to our designers

- Laser-fuses
- Electrically programmable fuses or anti-fuses
- Embedded OTP
- Embedded ROM
- Embedded SRAM with external ROM/Flash
- Natural, low-density, embedded Flash in standard CMOS, up to Kbits
- Embedded FPGAs
- Embedded mask-programmable sea-of-gates.

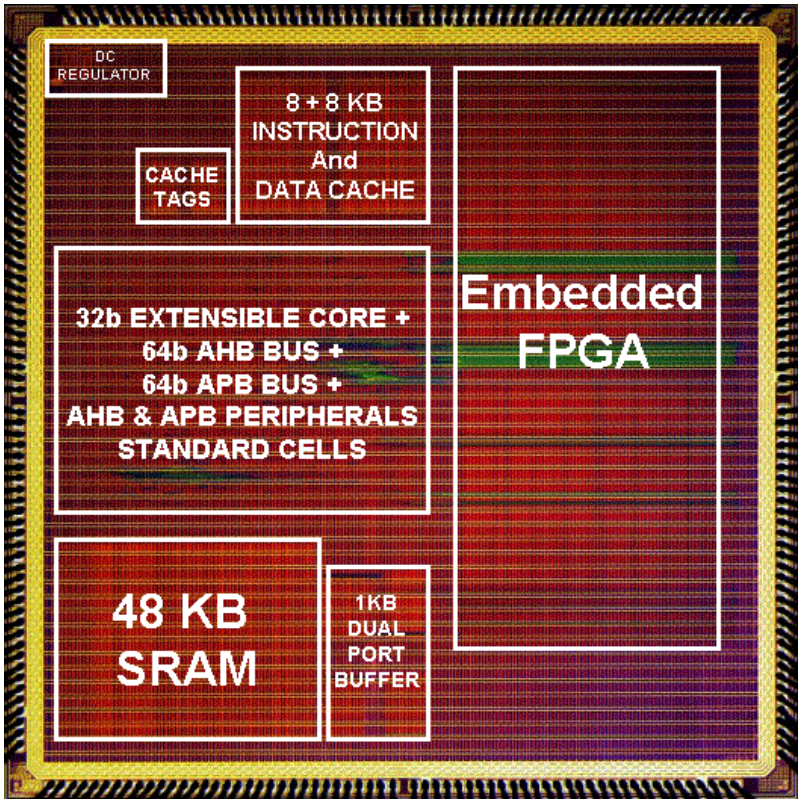
Reconfigurable IC with eASIC

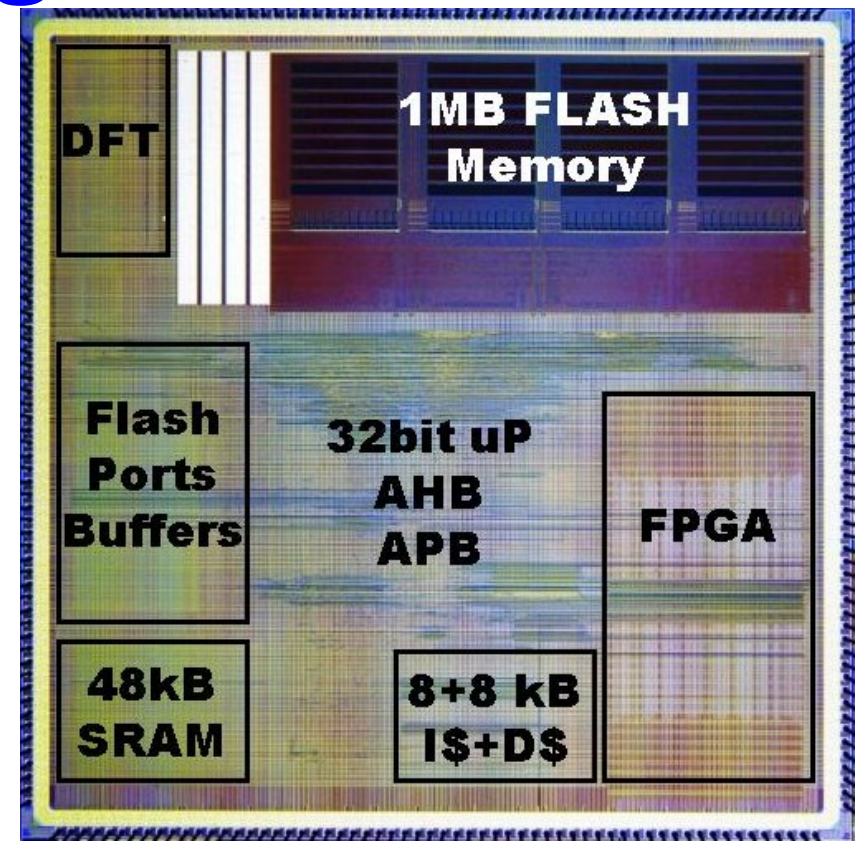


- 0.13um HCMOS9 technology
- Includes 12 eASICores (300k raw gates)
- Single-mask configuration

- Customization: 110k gates + 28kb DP-RAM
  - Area penalty: 3 - 3.5 x
  - Speed penalty: 2 - 2.5 x

eFPGA Reconfigurable SoC's





0.18um Working Silicon
Speed: 180 MHz
Average Power @ 50MHz: 140mW
-> in use in 0.13um

- 0.18um Working Silicon
- Speed: 110 MHz
- Average Power @50MHz: 160mW
- Paper at ISSCC 2003

The competition

TAIWAN

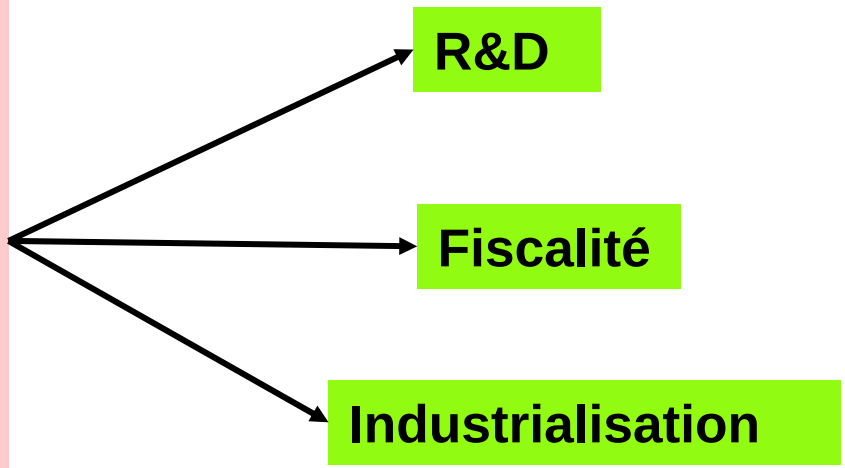
Un pays exemplaire :

•Ampleur et variété des formes d'aides

•Ampleur des résultats

9 secteurs prioritaires (plan de 1991)

- **Semi-conducteur**
- **Communication**
- Aérospatial
- **Informatique**
- **Précision machines et automatisation**
- **Advanced Materials Industry**
- Chimie et Pharmaceutique
- Médical
- Contrôle et traitement de la pollution



TAIWAN

TSMC, UMC, VANGUARD, VISHAY, …

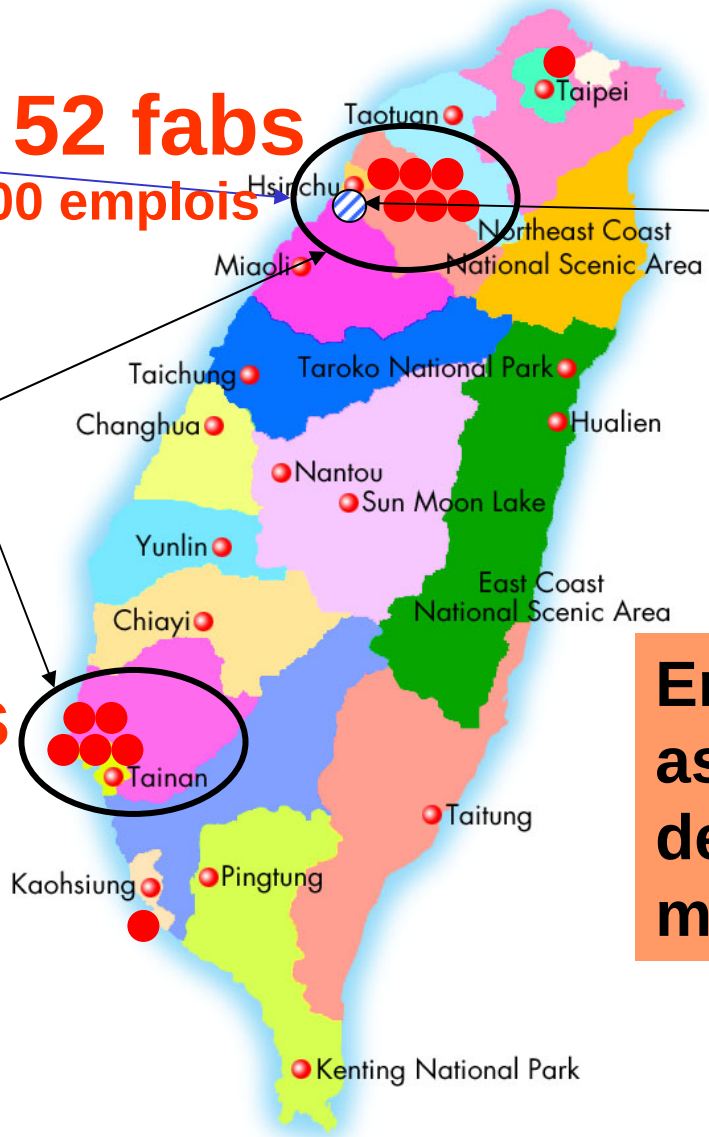
52 fabs

100 000 emplois

ITRI/ERSO

Parcs technologiques

10 fabs



En 2002, Taïwan assure près de 10% de la production mondiale

21 millions d'habitants

Centre de R&D

300 mm

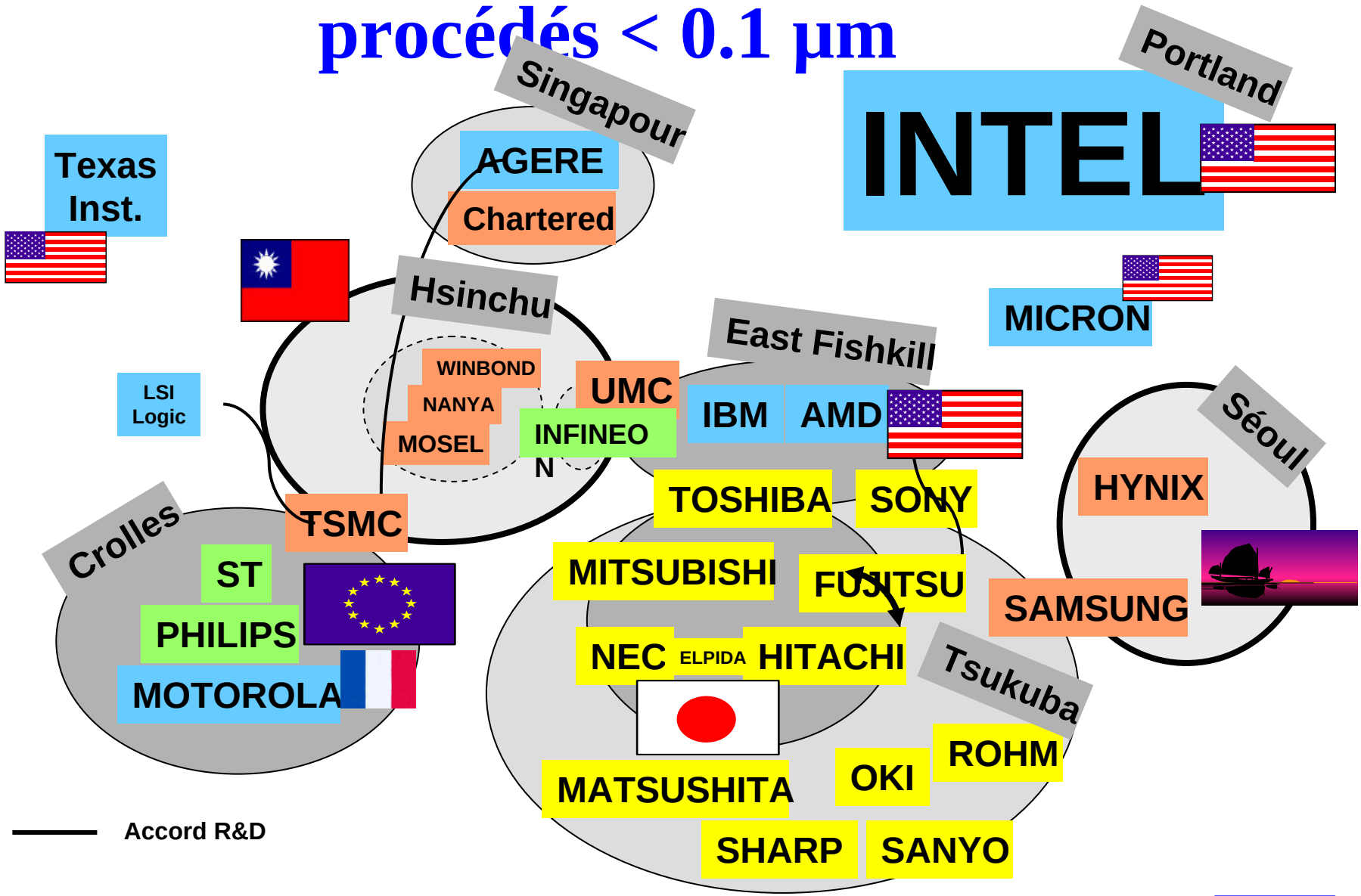
Fab universitaire/Labo public

Source : SEMI

Impact sur les entreprises taïwanaises

- Dépenses de R&D des grandes entreprises du semi-conducteur de Taiwan en 2000 :
  - **TSMC: 164 M$ (3% du CA) ,**
  - **UMC: 180 M$ (5% du CA),**
    soit moins de la moitié de ce qu'elles devraient être pour être en mesure avec leur chiffre d'affaires et leur activité.
- Mécanismes fiscaux pour déduire les investissements :
  - **Double déduction des investissements**
  - **Fiscalité réduite (exemption de 5 ans d'impôts sur les bénéfices)**

Alliances pour développements de procédés < 0.1 µm



Monsieur le President Jacques Chirac inaugure l'alliance Crolles2

Monsieur le President Jacques Chirac inaugure l'alliance Crolles2

Conclusions

- **Alliance and co-competition.**
- **Large portofolio of Technologies adapted to different SoC market needs: low power, high speed, RF, analog, imagers…**
- **Strong interactions between:**
  - Wafer Manufacturing
  - Technology Development
  - IP design
  - CAD Development
- **Low-power:**
  - Leakage is here to stay!!!
  - Design techniques / Process variants can help
  - More tools needed to predict/implement power solutions at all abstraction levels

Conclusions

- **Co-competition**

- **Low-power:**
  - Leakage is here to stay!!!
  - Design techniques / Process variants can help
  - More tools needed to predict/implement power solutions at all abstraction levels